EE 330
Lecture 11

Copper Interconnects

Resistance and Capacitance in Interconnects

Fall 2023 Exam Schedule

Exam 1	Friday Sept 22	
Exam 2	Friday Oct 20	
Exam 3	Friday Nov. 17	
Final	Monday Dec 11	12:00 – 2:00 p.m.

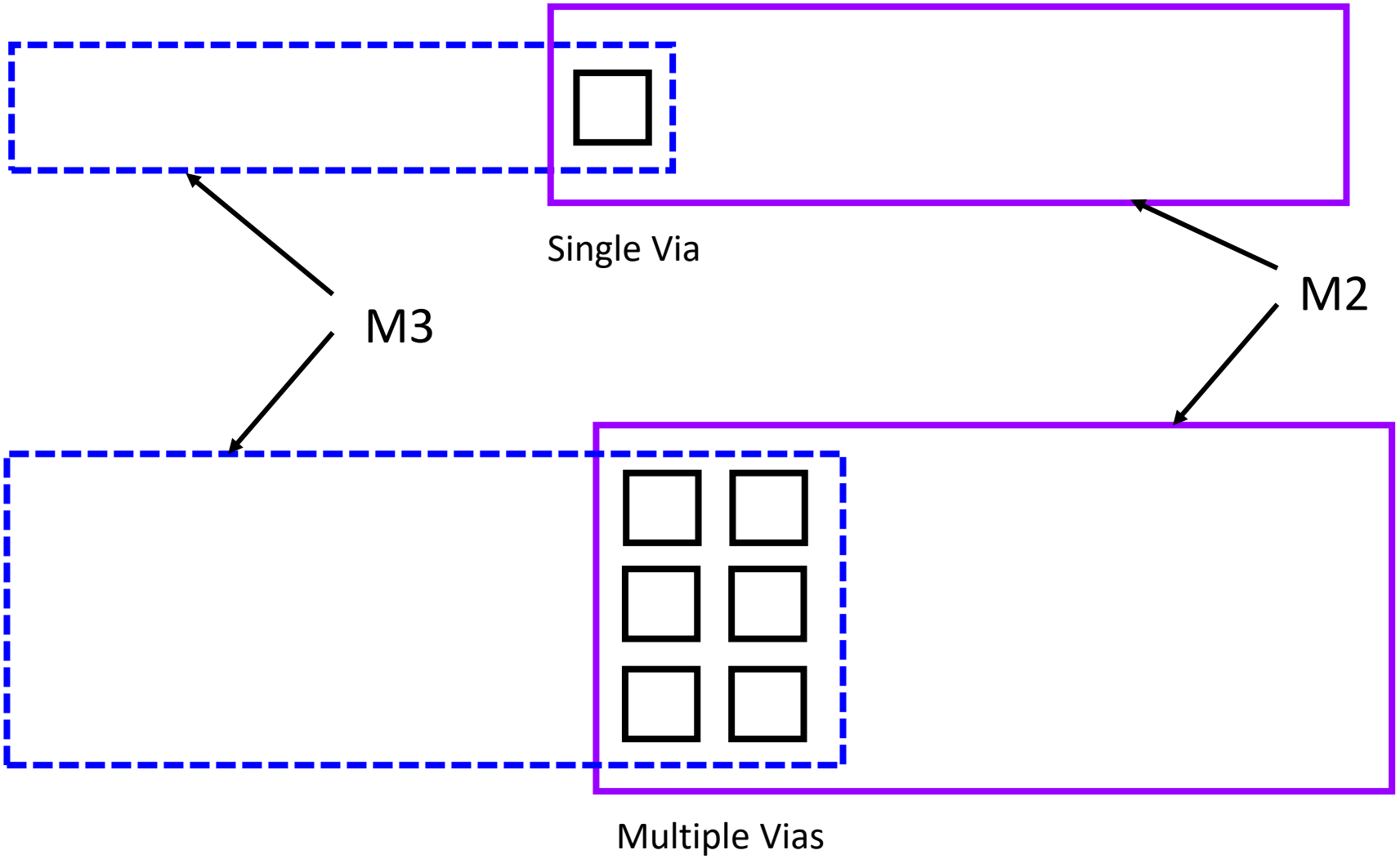
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Ion Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Planarization
- Contacts, Interconnect and Metalization

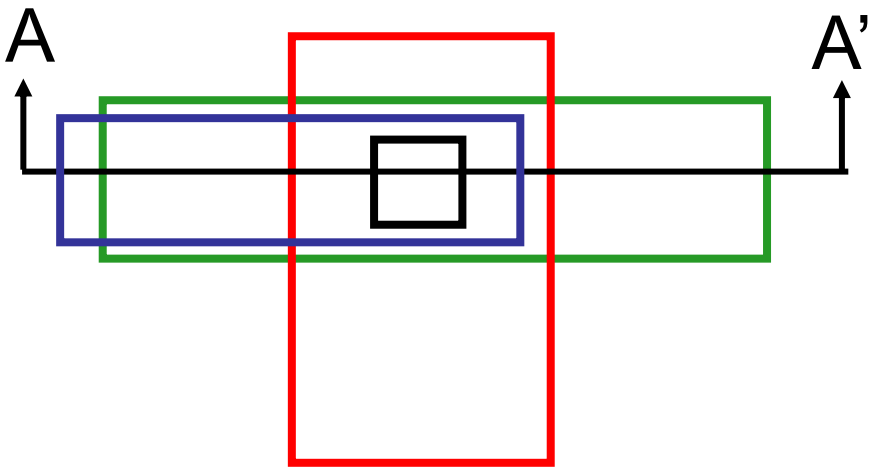
Contacts, Interconnect and Metallization

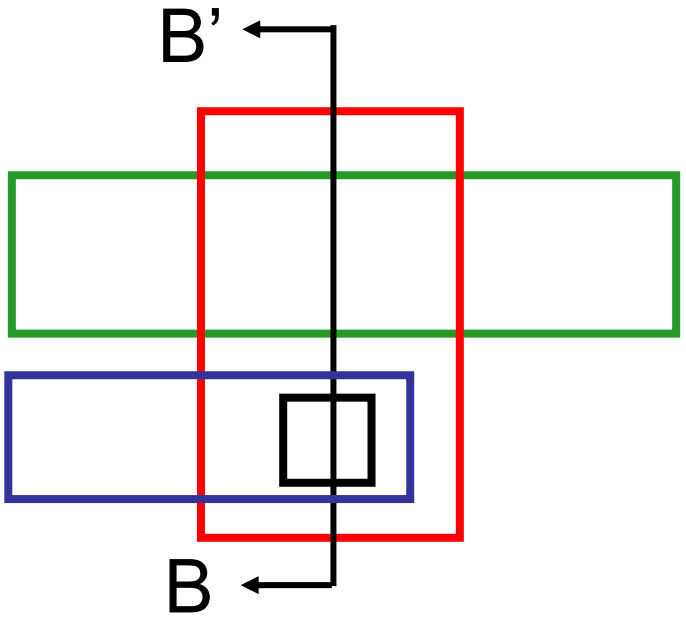
- Contacts (vias) used to identify where vertically stacked layers connect
- Contacts (vias) used to identify which vertically stacked layers connect
- Term “vias” usually refers to metal-metal connections and “contact” where one layer is not metal
- Contacts and vias usually of a fixed size
  - All etches reach bottom at about the same time
  - Multiple contacts widely used (to reduce resistance)
  - Contacts not allowed to Poly on thin oxide in most processes
  - Dog-bone often needed for minimum-length devices
  - Vias usually only allowed between adjacent metal layers

Vias

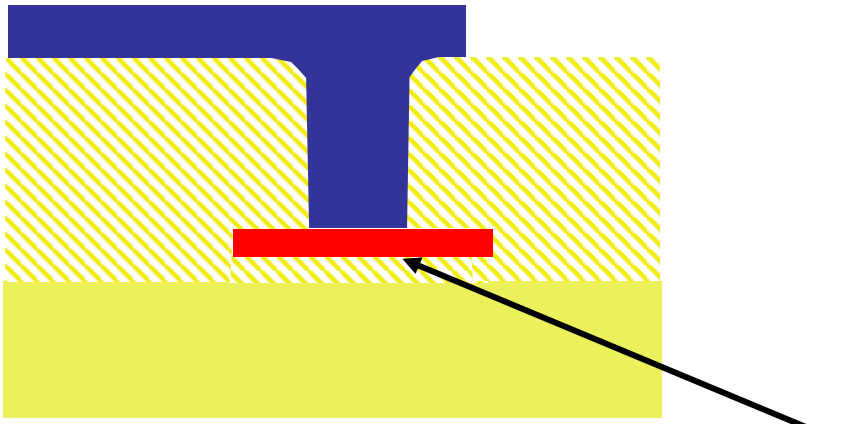


Contacts





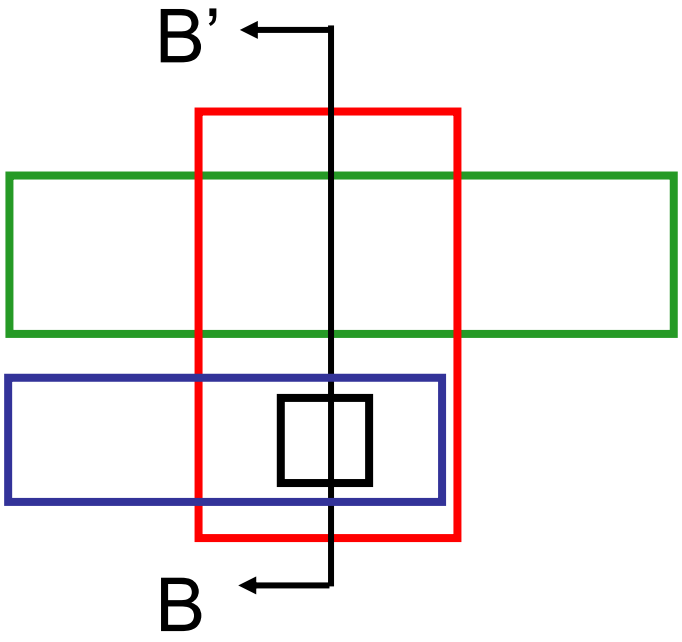
Acceptable Metal-Poly Contact

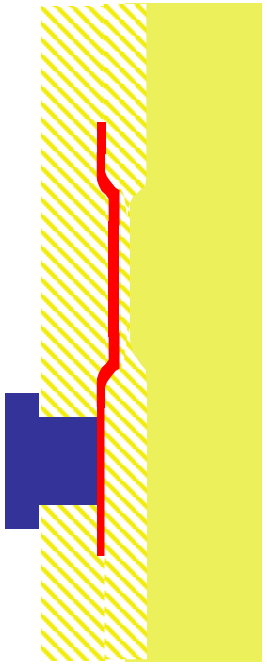


Unacceptable Metal-Poly Contact

Vulnerable to pin holes
(usually all contacts are same size)

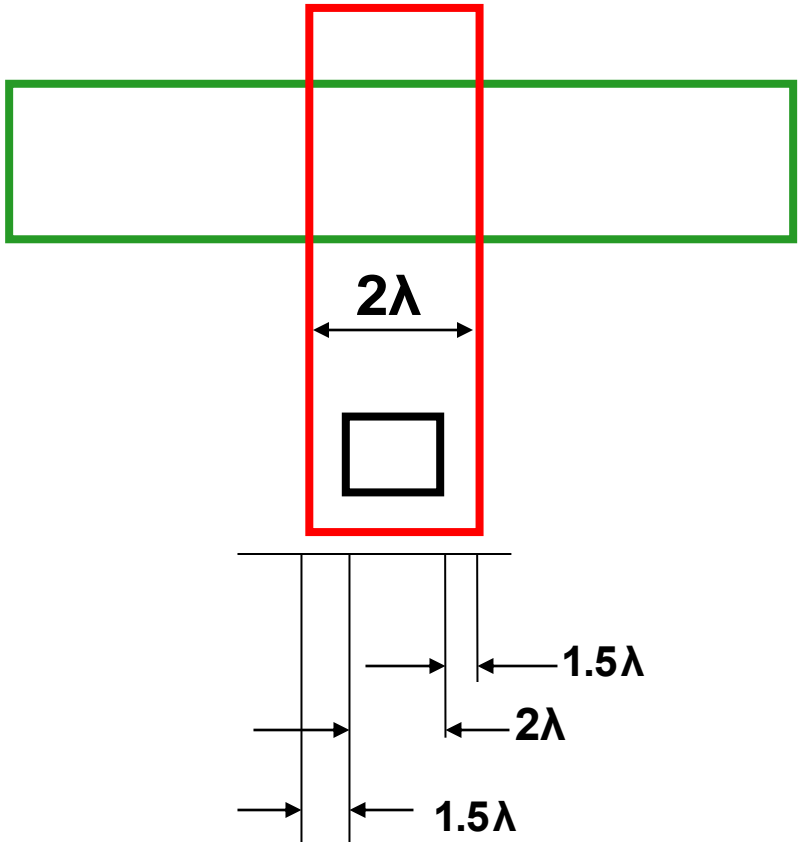
Contacts



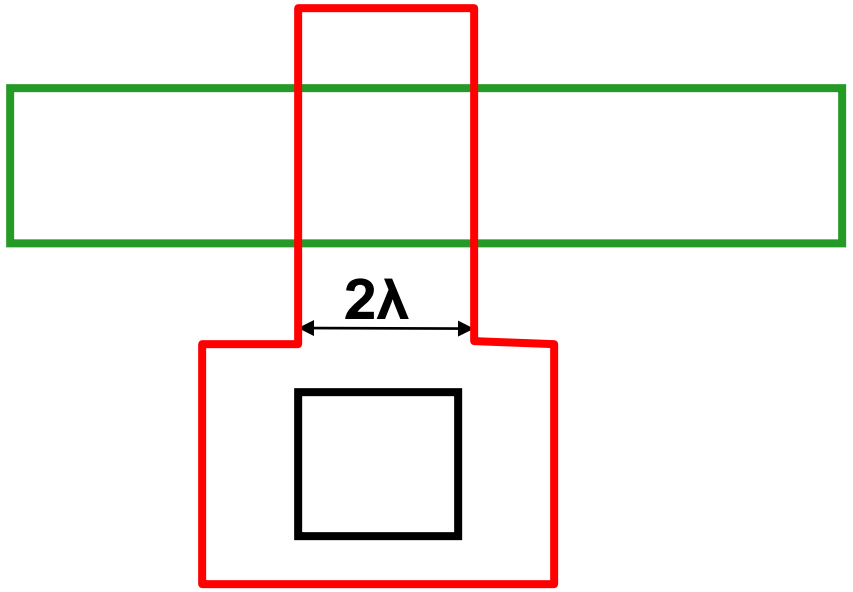


Acceptable Metal-Poly Contact

Contacts

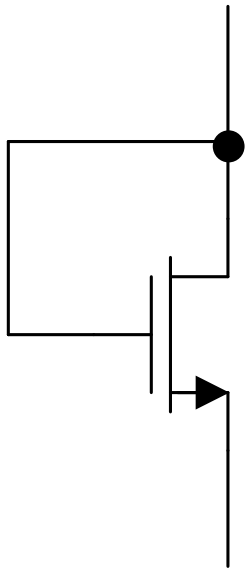


Design Rule Violation

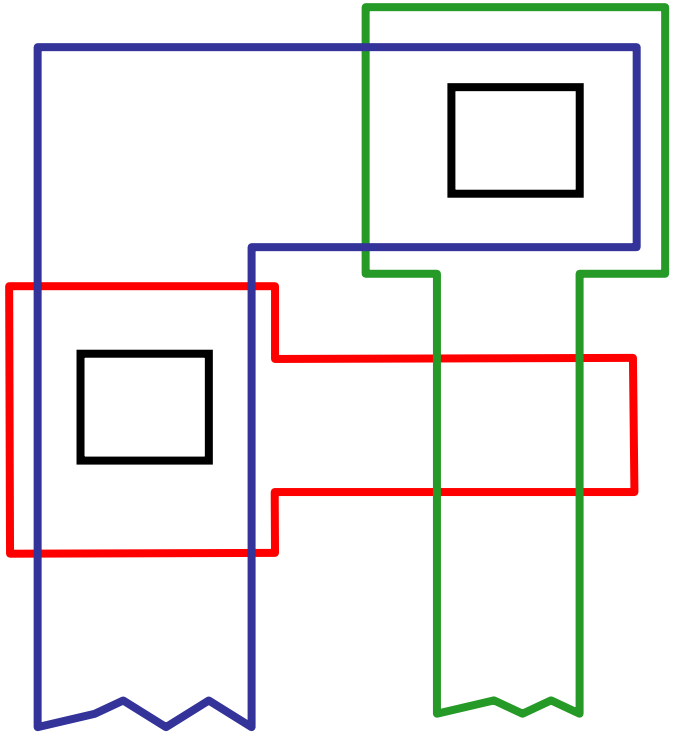


“Dog Bone” Contact

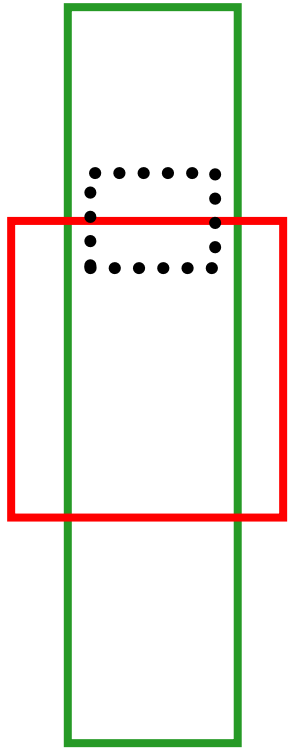
Contacts



Common
Circuit
Connection



Standard Interconnection



Buried Contact

Can save area but not
allowed in many processes

Metalization

- Aluminum widely used for interconnect
- Copper often replacing aluminum in recent processes
- Must not exceed maximum current density
  - around 1ma/u for aluminum and copper
- Ohmic Drop must be managed
- Parasitic Capacitances must be managed
- Interconnects from high to low level metals require connections to each level of metal
- Stacked vias permissible in some processes

Metalization

Aluminum

- Aluminum is usually deposited uniformly over entire surface and etched to remove unwanted aluminum
- Mask is used to define area in photoresist where aluminum is to be removed

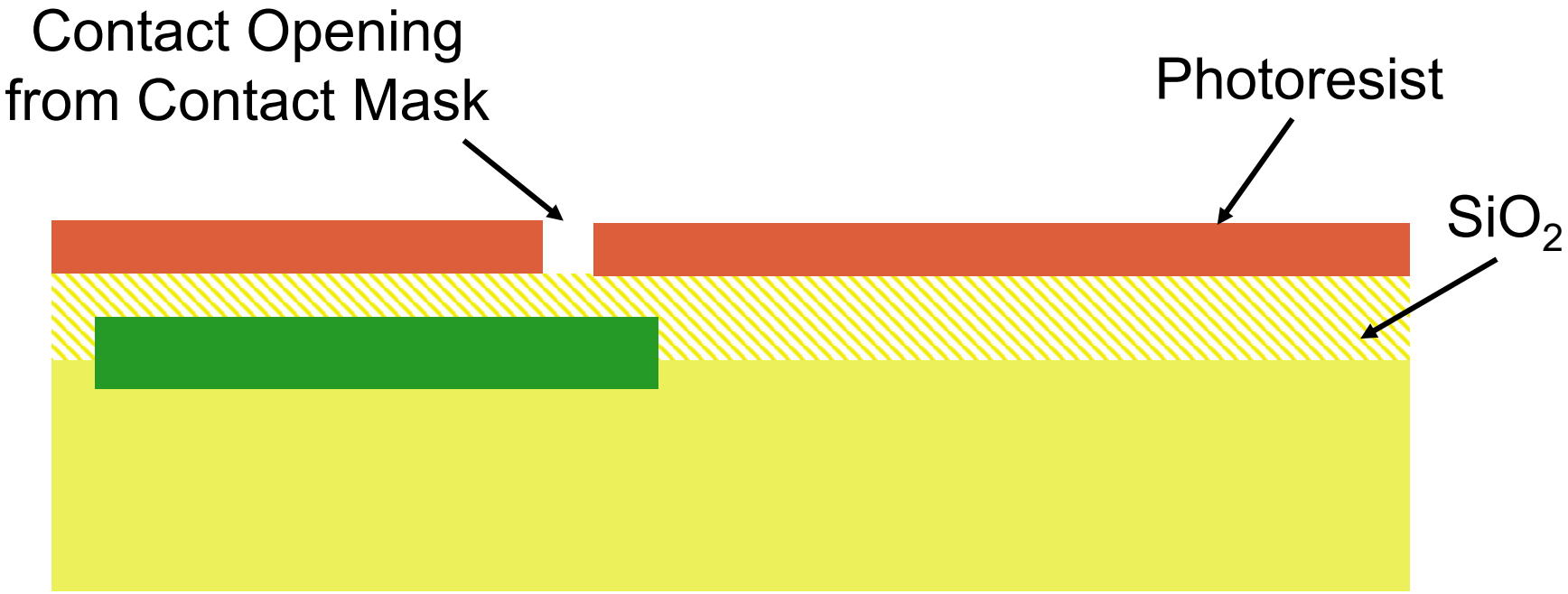
Copper

- Plasma etches not effective at removing copper because of absence of volatile copper compounds
- Barrier metal layers needed to isolate silicon from migration of copper atoms
- Damascene or Dual-Damascene processes used to pattern copper

Patterning of Aluminum

Consider Metal 1 (lowest level of metal)

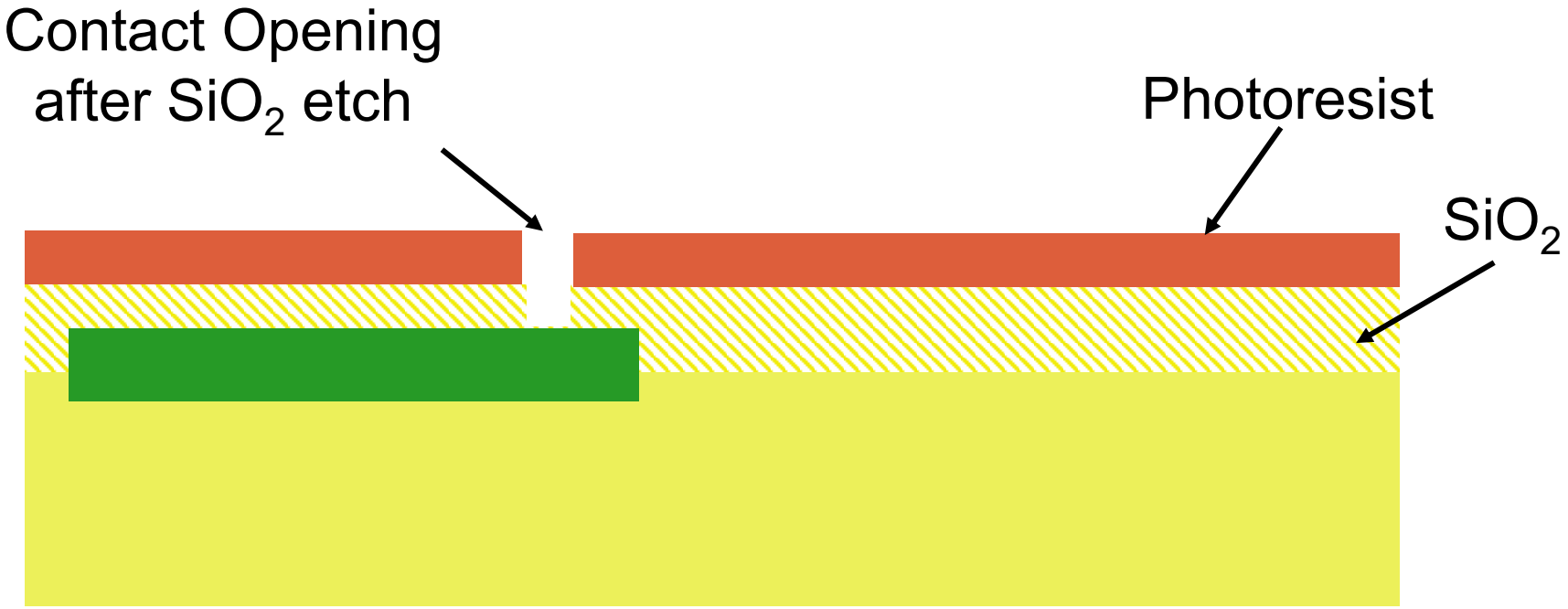
- Will contact to n-active
- Consider process with LOCOS



Patterning of Aluminum

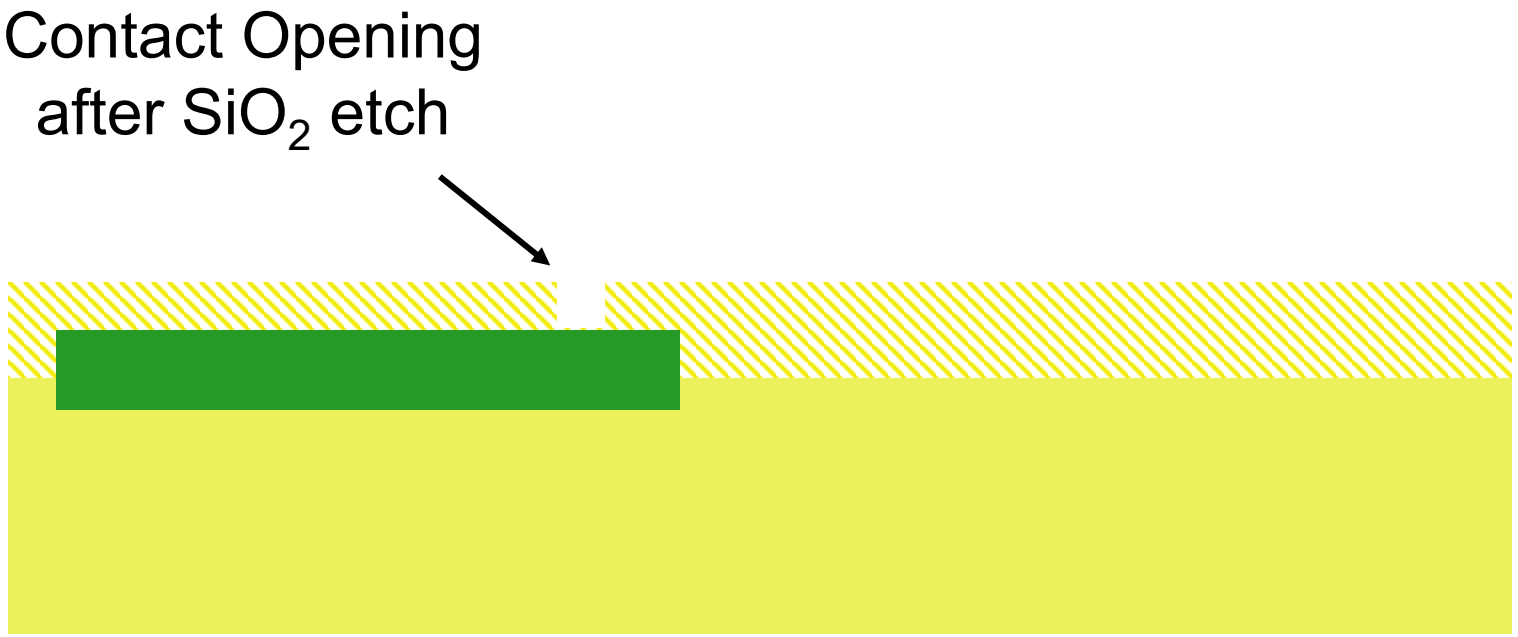
Consider Metal 1 (lowest level of metal)

- Will contact to n-active
- Consider process with LOCOS



Patterning of Aluminum

Consider Metal 1 (lowest level of metal)

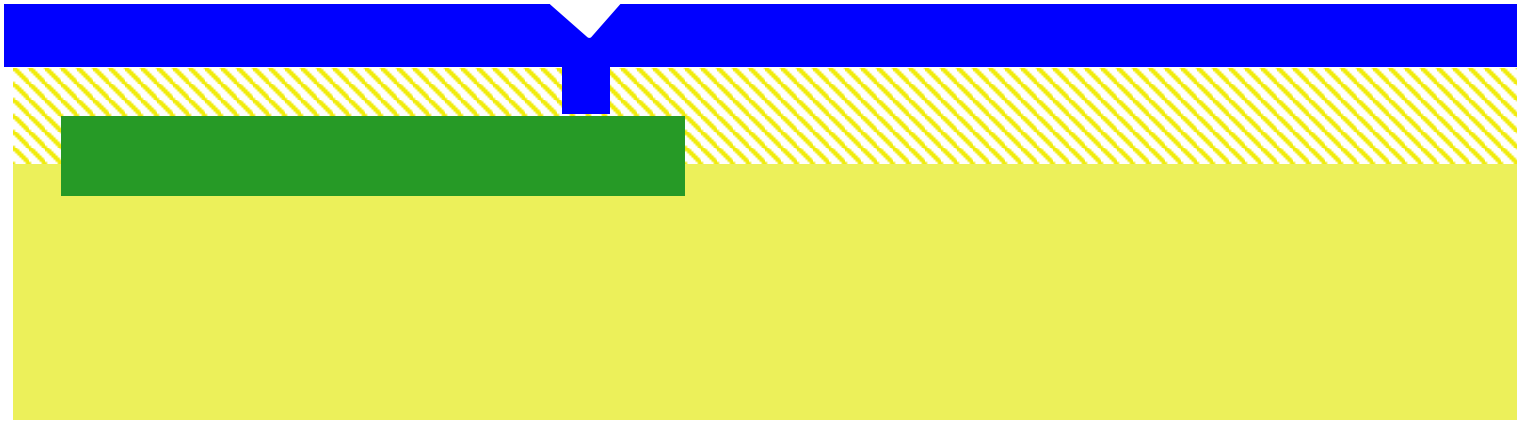


After Photoresist Removed

Patterning of Aluminum

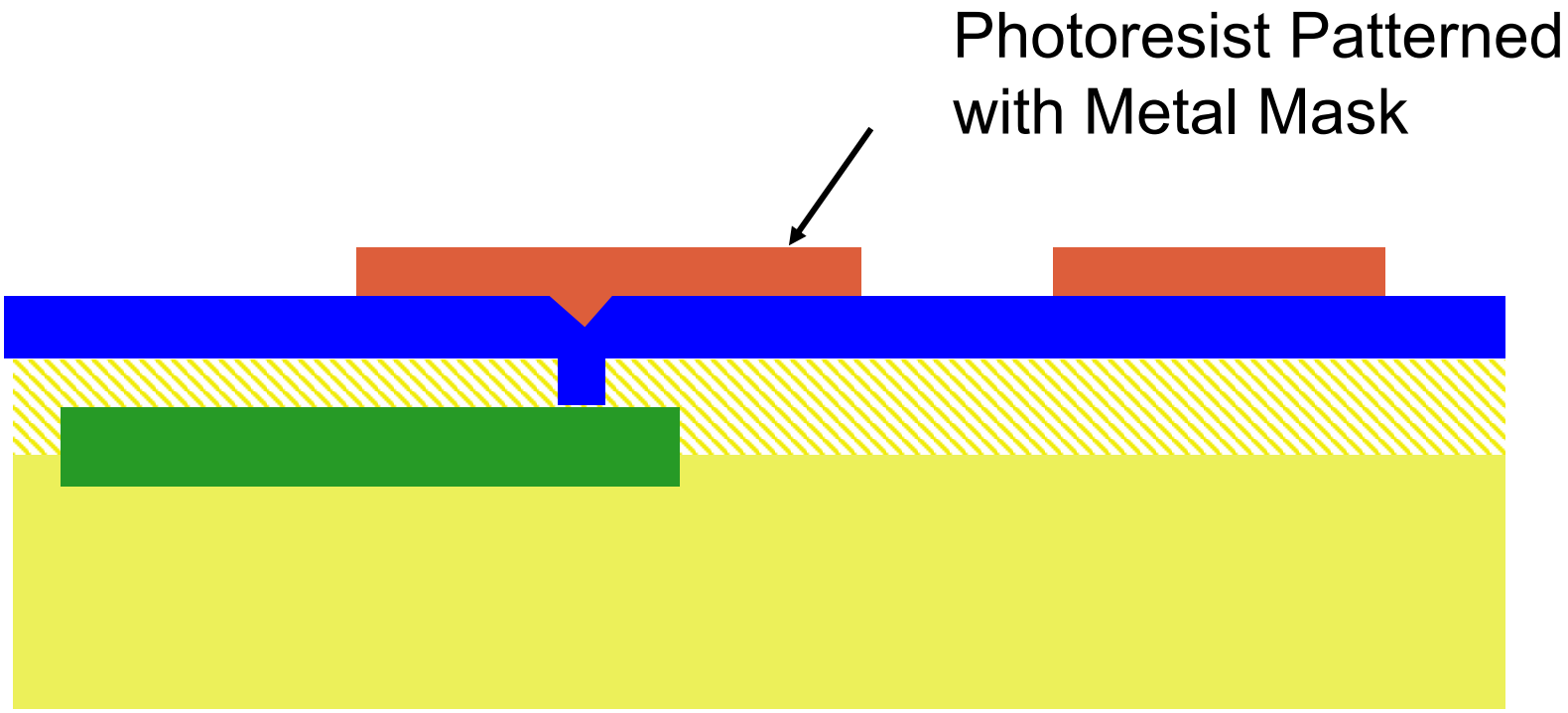
Consider Metal 1 (lowest level of metal)

Metal Applied to Entire Surface



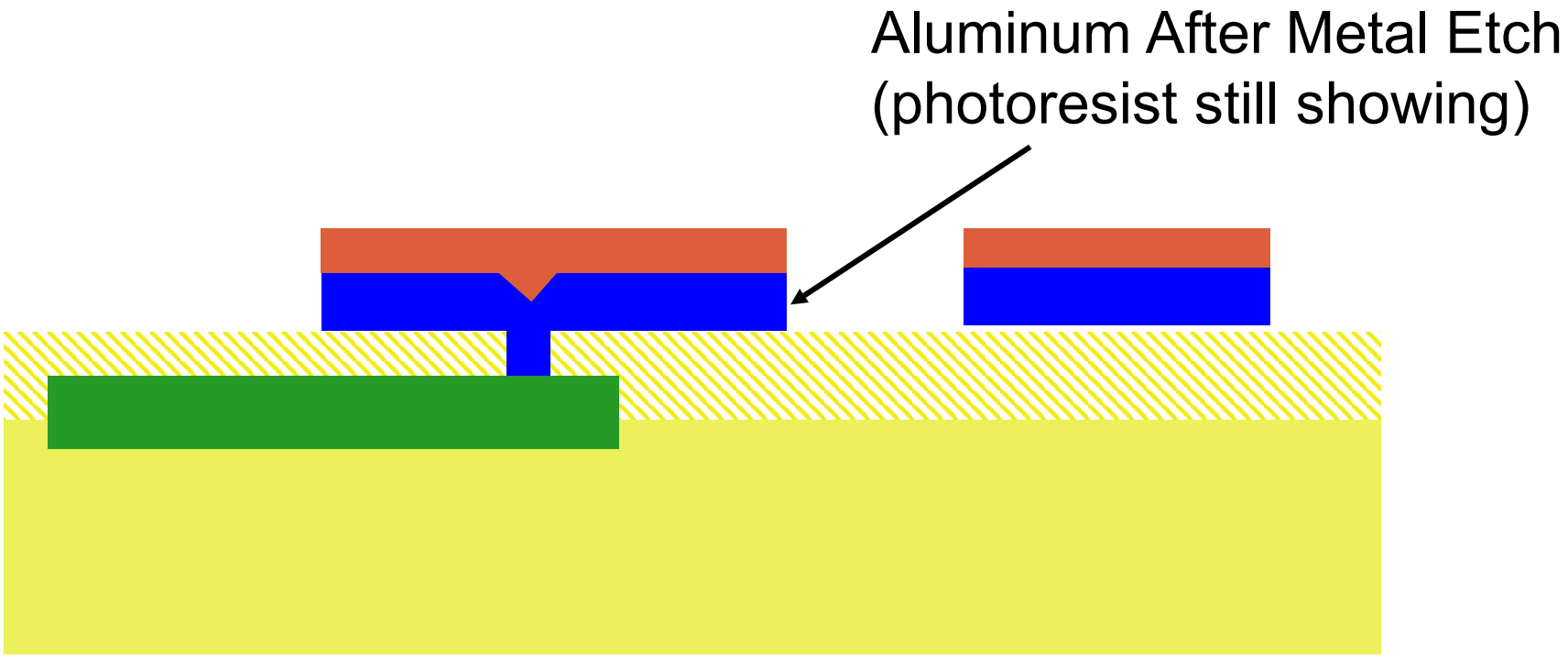
Patterning of Aluminum

Consider Metal 1 (lowest level of metal)



Patterning of Aluminum

Consider Metal 1 (lowest level of metal)



Copper Interconnects

Limitations of Aluminum Interconnects

- Electromigration
- Conductivity not real high

Relevant Key Properties of Copper

- Reduced electromigration problems at given current level
- Better conductivity

Challenges of Copper Interconnects

- Absence of volatile copper compounds (can not use plasma etch)
- Copper diffuses into surrounding materials (barrier metal required)

Material	ρ (Ω·m) at 20 °C	σ (S/m) at 20 °C	Temperat coefficient[(K^{-1})
Carbon (graphene)	1.00×10^{-8}	1.00×10^{8}	−0.0002
Silver	1.59×10^{-8}	6.30×10^{7}	0.0038
Copper	1.68×10^{-8}	5.96×10^{7}	0.003862
Annealed copper[note 2]	1.72×10^{-8}	5.80×10^{7}	0.00393
Gold[note 3]	2.44×10^{-8}	4.10×10^{7}	0.0034
Aluminium[note 4]	2.82×10^{-8}	3.50×10^{7}	0.0039
Calcium	3.36×10^{-8}	2.98×10^{7}	0.0041
Tungsten	5.60×10^{-8}	1.79×10^{7}	0.0045
Zinc	5.90×10^{-8}	1.69×10^{7}	0.0037
Nickel	6.99×10^{-8}	1.43×10^{7}	0.006
Lithium	9.28×10^{-8}	1.08×10^{7}	0.006
Iron	9.71×10^{-8}	1.00×10^{7}	0.005
Platinum	1.06×10^{-7}	9.43×10^{6}	0.00392
Tin	1.09×10^{-7}	9.17×10^{6}	0.0045
Carbon steel (1010)	1.43×10^{-7}	6.99×10^{6}	

Source:
Sept 13, 2017

Lead	2.20×10^{-7}	4.55×10^{6}	0.0039
Titanium	4.20×10^{-7}	2.38×10^{6}	0.0038
Grain oriented electrical steel	4.60×10^{-7}	2.17×10^{6}	
Manganin	4.82×10^{-7}	2.07×10^{6}	0.000002
Constantan	4.90×10^{-7}	2.04×10^{6}	0.000008
Stainless steel[note 5]	6.90×10^{-7}	1.45×10^{6}	0.00094
Mercury	9.80×10^{-7}	1.02×10^{6}	0.0009
Nichrome[note 6]	1.10×10^{-6}	6.7×10^{5}	0.0004
GaAs	1.00×10^{-3} to 1.00×10^{8}	1.00×10^{-8} to 10^{3}	
Carbon (amorphous)	5.00×10^{-4} to 8.00×10^{-4}	1.25×10^{3} to 2×10^{3}	−0.0005
Carbon (graphite)[note 7]	2.50×10^{-6} to 5.00×10^{-6} ∥basal plane 3.00×10^{-3} ⊥basal plane	2.00×10^{5} to 3.00×10^{5} ∥basal plane 3.30×10^{2} ⊥basal plane	
PEDOT:PSS	2×10^{-6} to 1×10^{-1}	1×10^{1} to 4.6×10^{5}	?
Germanium[note 8]	4.60×10^{-1}	2.17	−0.048
Sea water[note 9]	2.00×10^{-1}	4.80	
Swimming pool water[note 10]	3.33×10^{-1} to 4.00×10^{-1}	0.25 to 0.30	

Silicon[note 8]	6.40×10^{2}	1.56×10^{-3}	−0.075
Wood (damp)	1.00×10^{3} to 1.00×10^{4}	10^{-4} to 10^{-3}	
Deionized water[note 12]	1.80×10^{5}	5.50×10^{-6}	
Glass	1.00×10^{11} to 1.00×10^{15}	10^{-15} to 10^{-11}	?
Hard rubber	1.00×10^{13}	10^{-14}	?
Wood (oven dry)	1.00×10^{14} to 1.00×10^{16}	10^{-16} to 10^{-14}	
Sulfur	1.00×10^{15}	10^{-16}	?
Air	1.30×10^{14} to 3.30×10^{14}	3×10^{-15} to 8×10^{-15}	
Carbon (diamond)	1.00×10^{12}	$\sim 10^{-13}$	
Fused quartz	7.50×10^{17}	1.30×10^{-18}	?
PET	1.00×10^{21}	10^{-21}	?
Teflon	1.00×10^{23} to 1.00×10^{25}	10^{-25} to 10^{-23}	?

Copper Interconnects

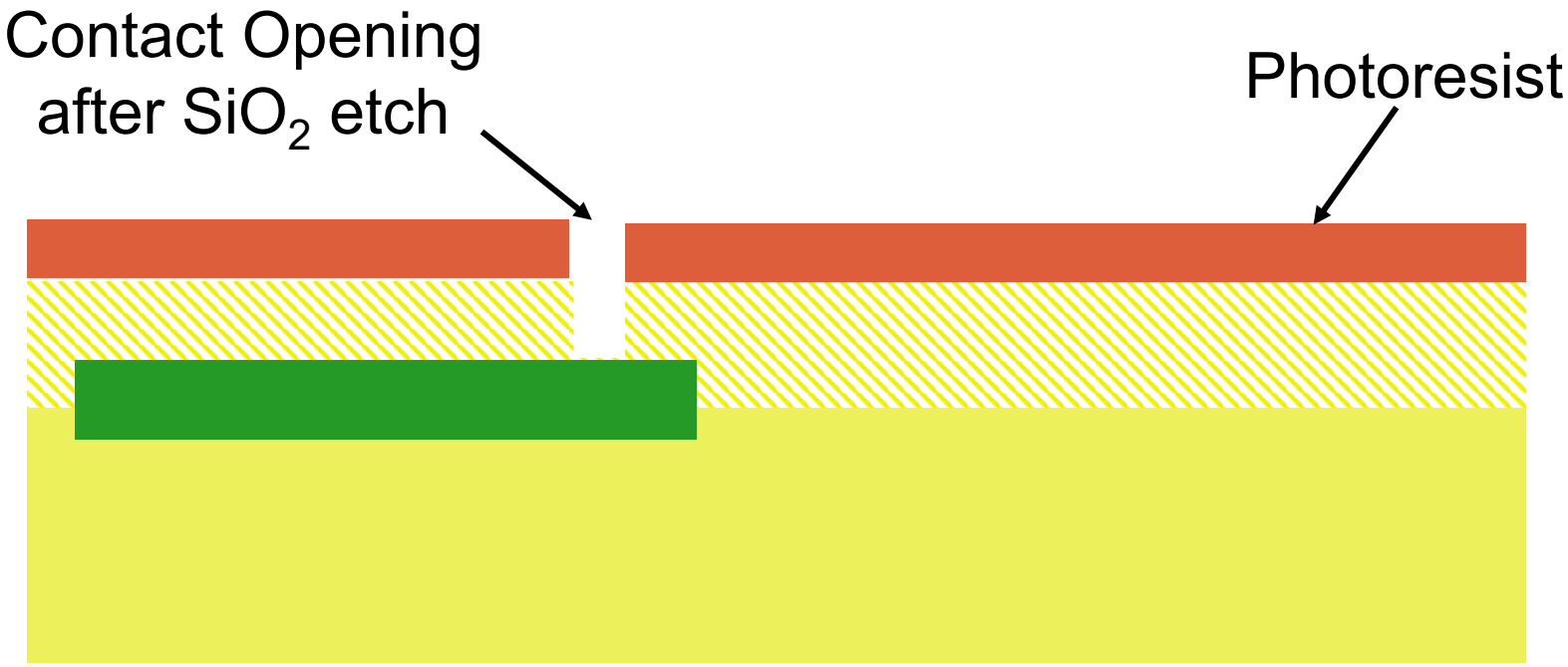
Practical methods of realizing copper interconnects took many years to develop

Copper interconnects widely used in some processes today

Patterning of Copper

Consider Metal 1 (lowest level of metal)

Damascene Process

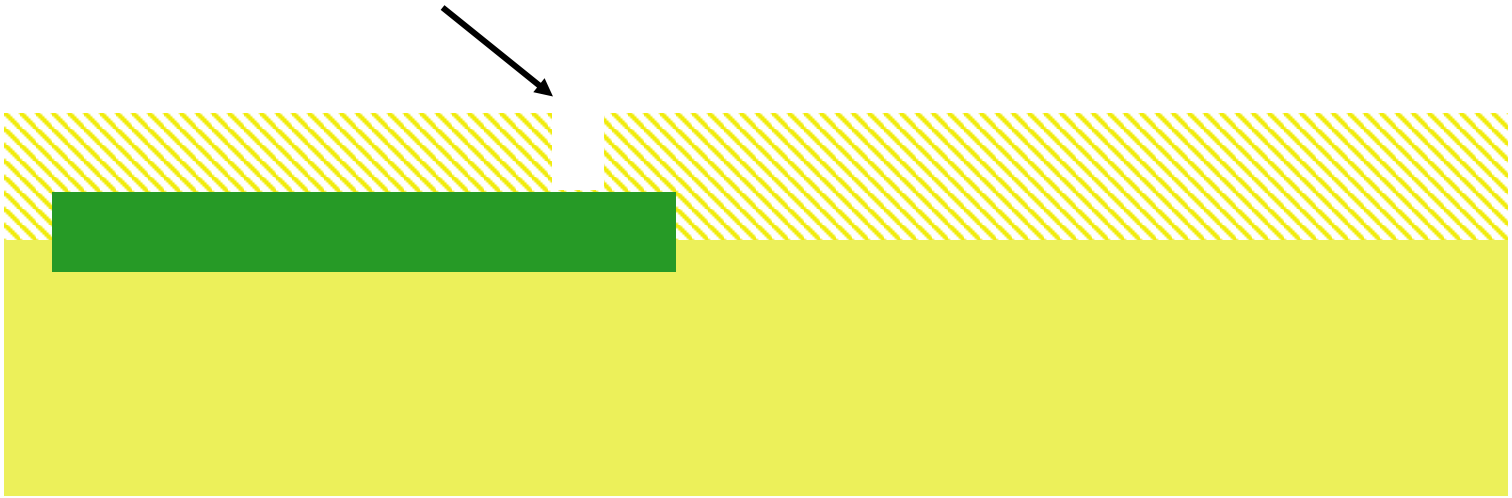


Patterning of Copper

Consider Metal 1 (lowest level of metal)

Damascene Process

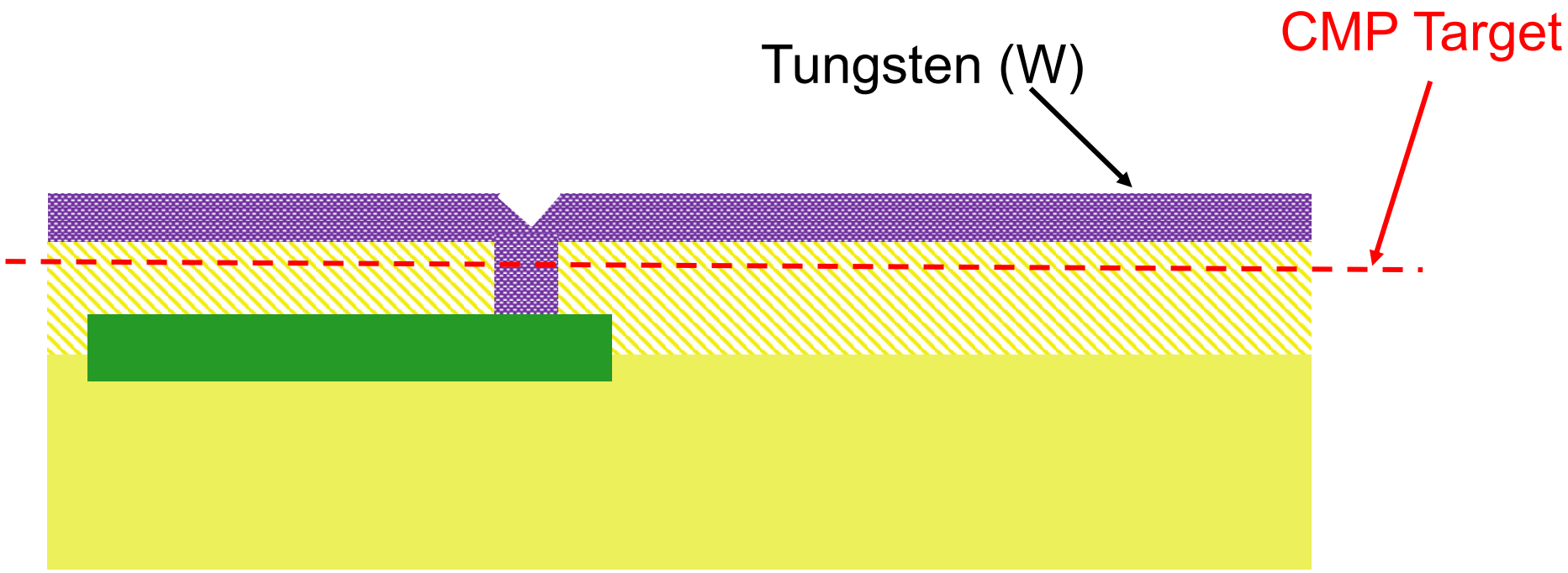
Contact Opening
after SiO_2 etch



Patterning of Copper

Consider Metal 1 (lowest level of metal)

Damascene Process

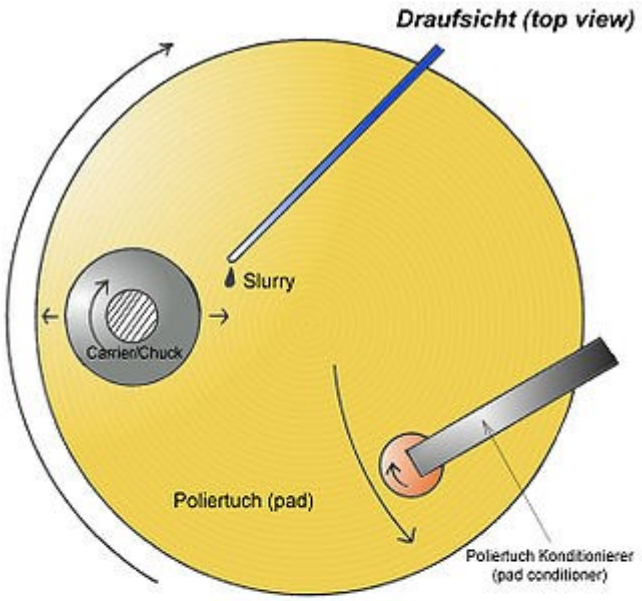


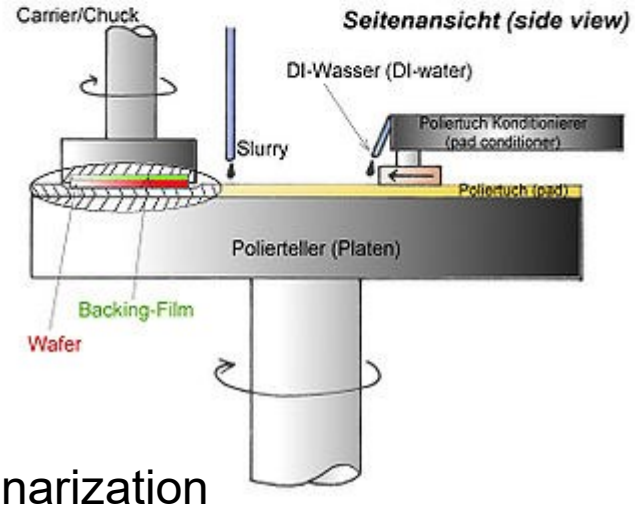
W has excellent conformality when formed from WF_6

Applied with CVD $WF_6+3H_2 \rightarrow W+6HF$

Chemical-Mechanical Planarization (CMP)

- Polishing Pad and Wafer Rotate in non-concentric pattern to thin, polish, and planarize surface
- Abrasive/Chemical polishing
- Depth and planarity are critical





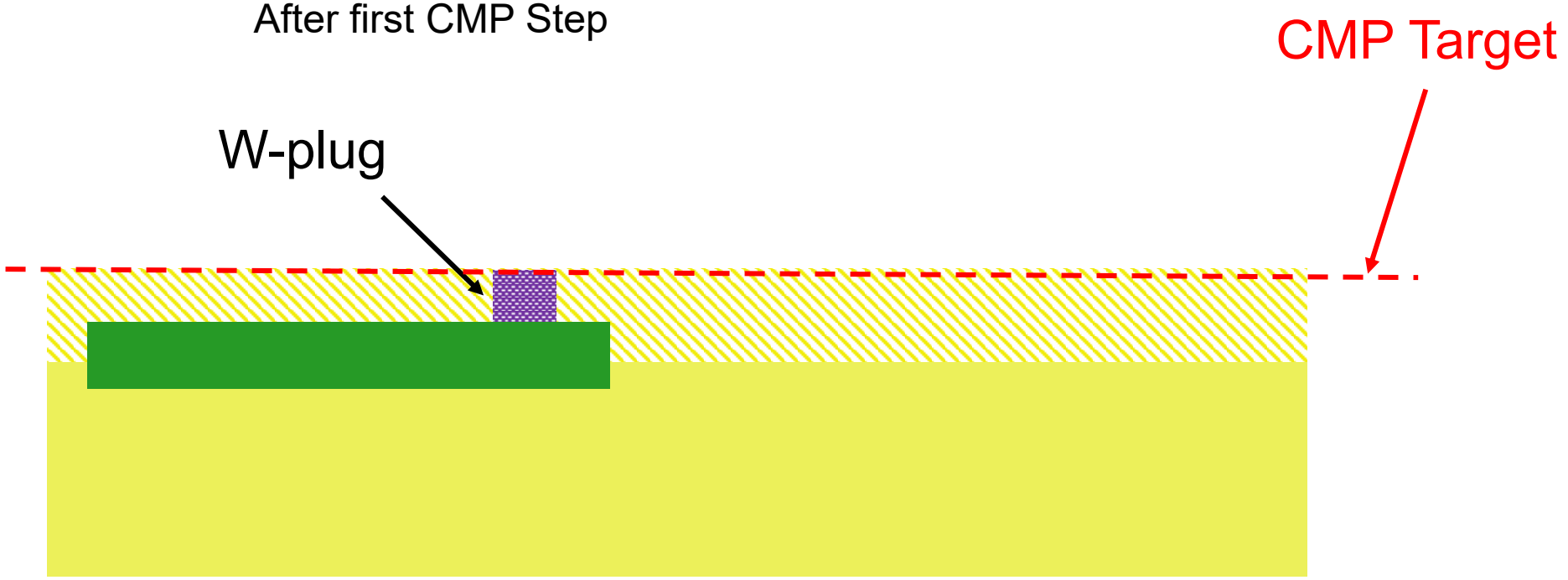
Acknowledgement:
http://en.wikipedia.org/wiki/Chemical-mechanical_planarization

Patterning of Copper

Consider Metal 1 (lowest level of metal)

Damascene Process

After first CMP Step



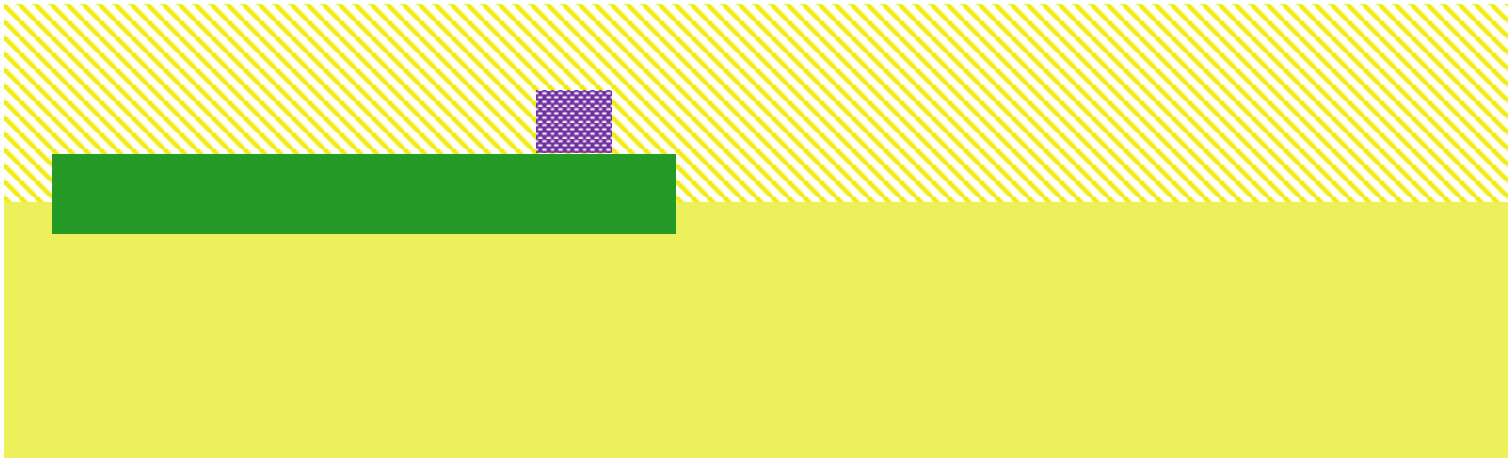
Patterning of Copper

Consider Metal 1 (lowest level of metal)

Damascene Process

After first CMP Step

Oxidation

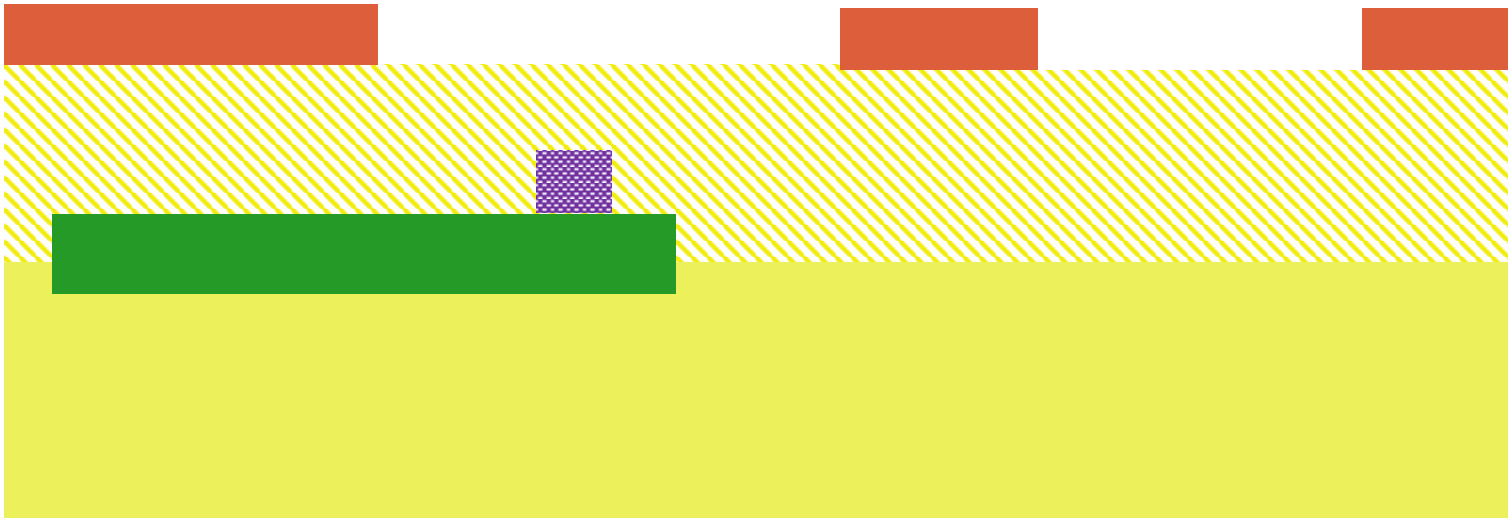


Patterning of Copper

Consider Metal 1 (lowest level of metal)

Damascene Process

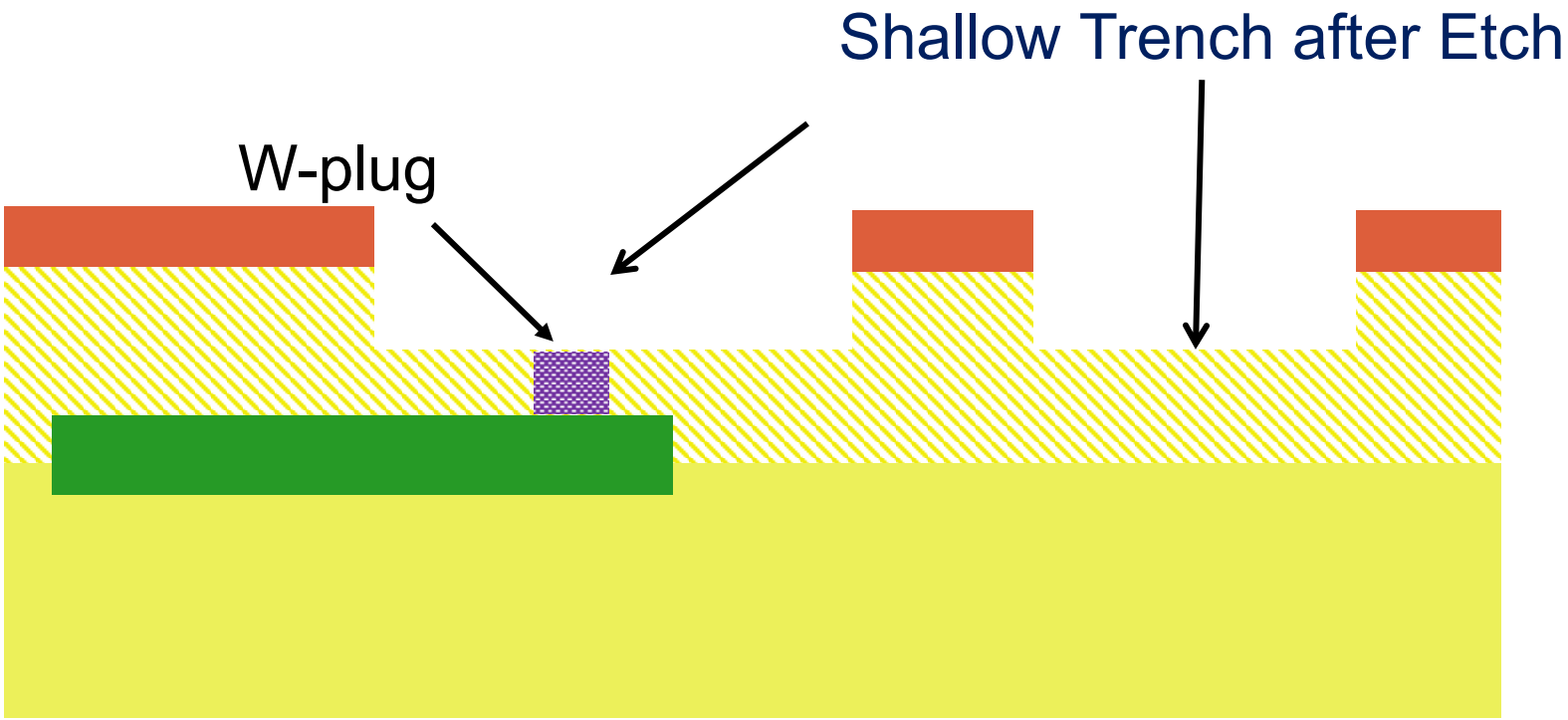
Photoresist Patterned with
Metal Mask Defines Trench



Patterning of Copper

Consider Metal 1 (lowest level of metal)

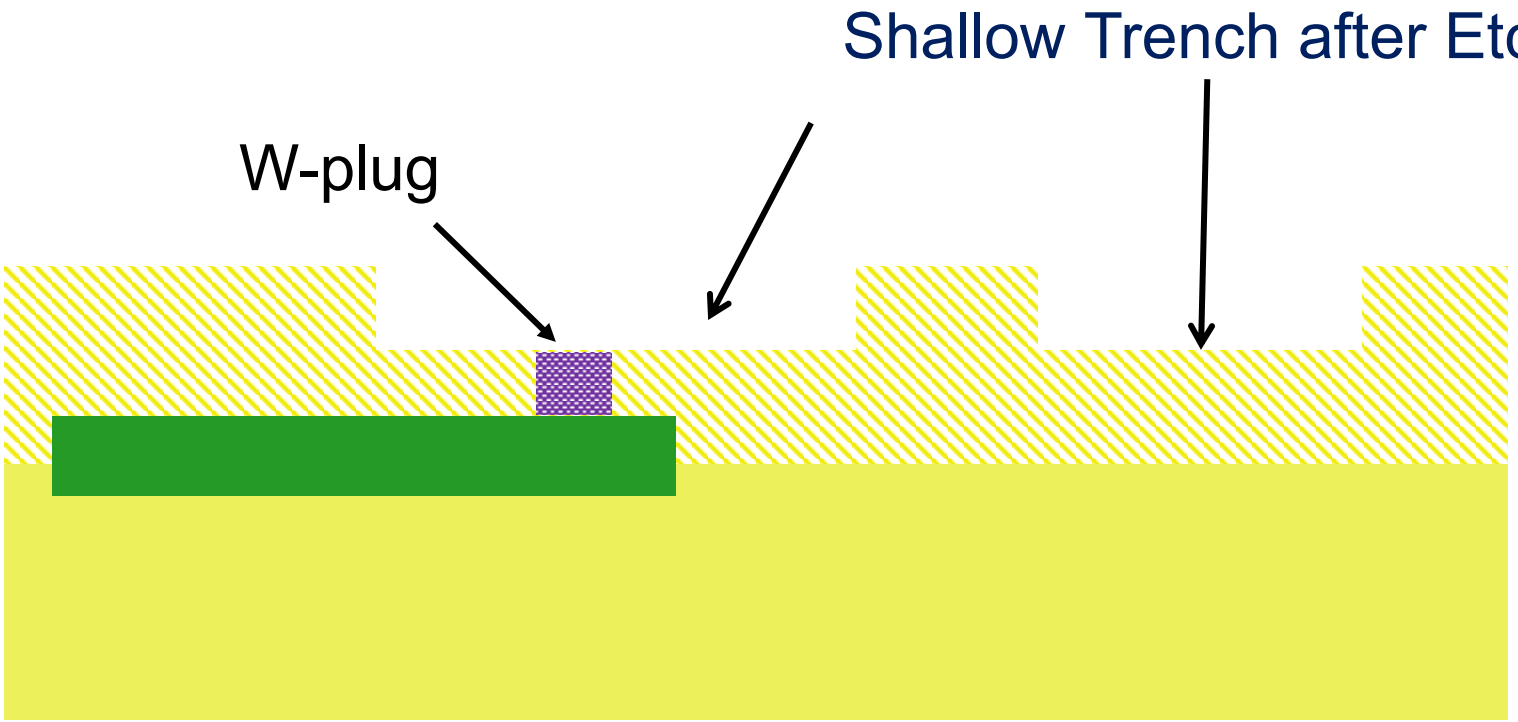
Damascene Process



Patterning of Copper

Consider Metal 1 (lowest level of metal)

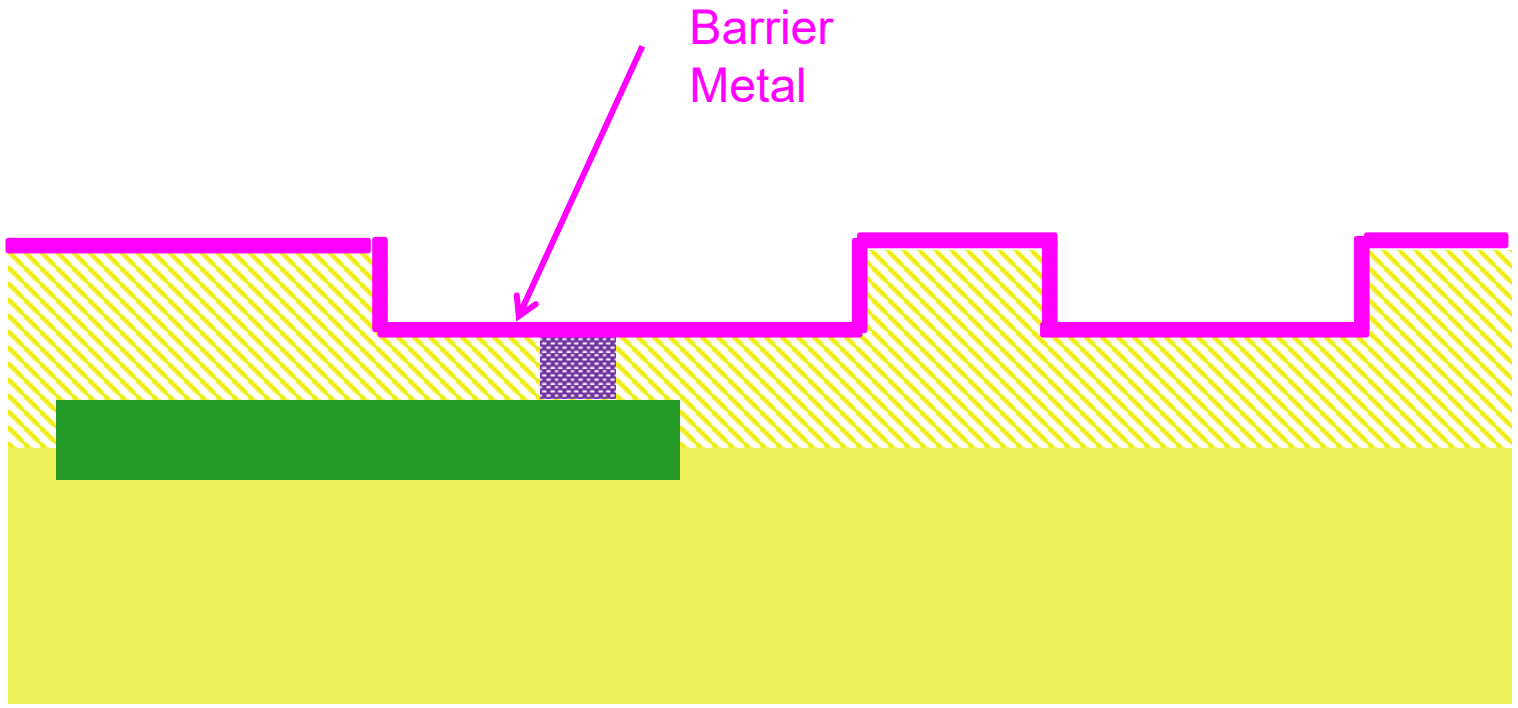
Damascene Process



Patterning of Copper

Consider Metal 1 (lowest level of metal)

Damascene Process

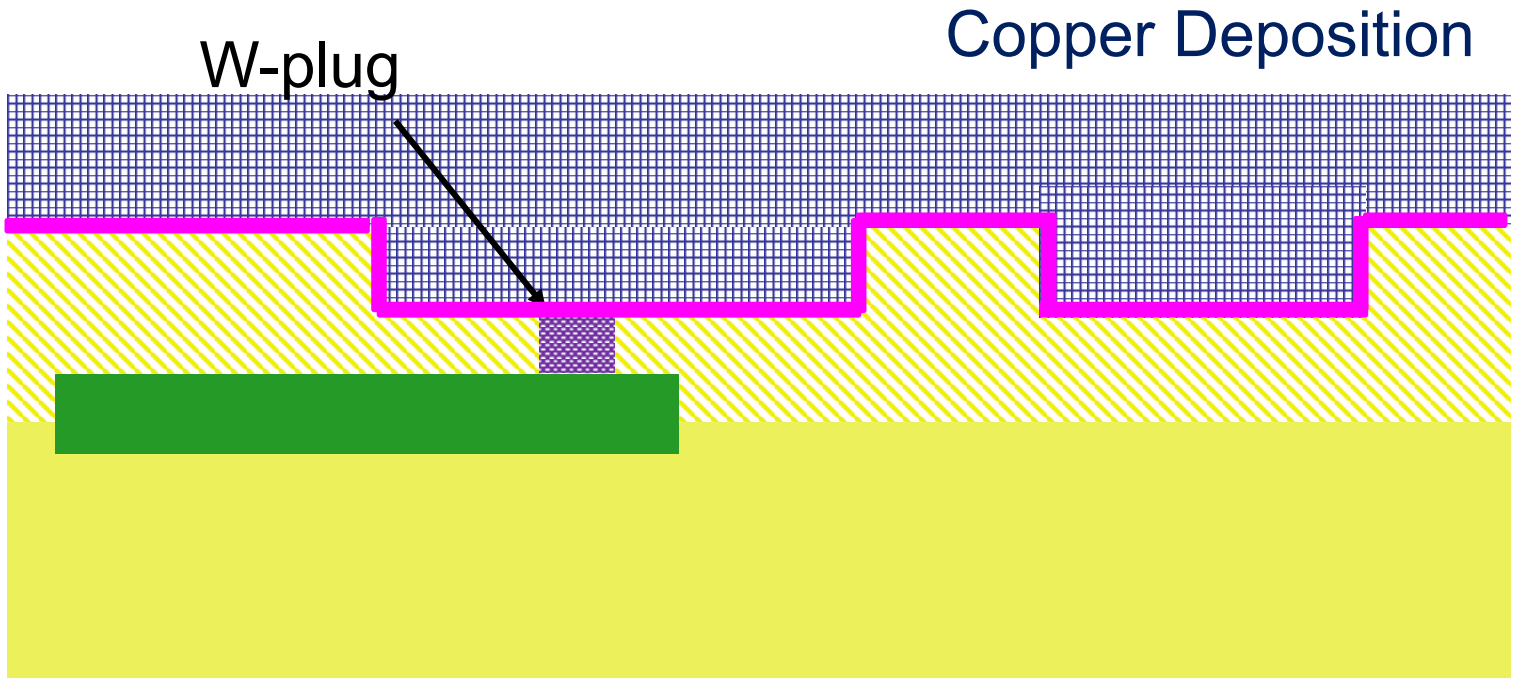


(Barrier metal added before copper to contain the copper atoms)

Patterning of Copper

Consider Metal 1 (lowest level of metal)

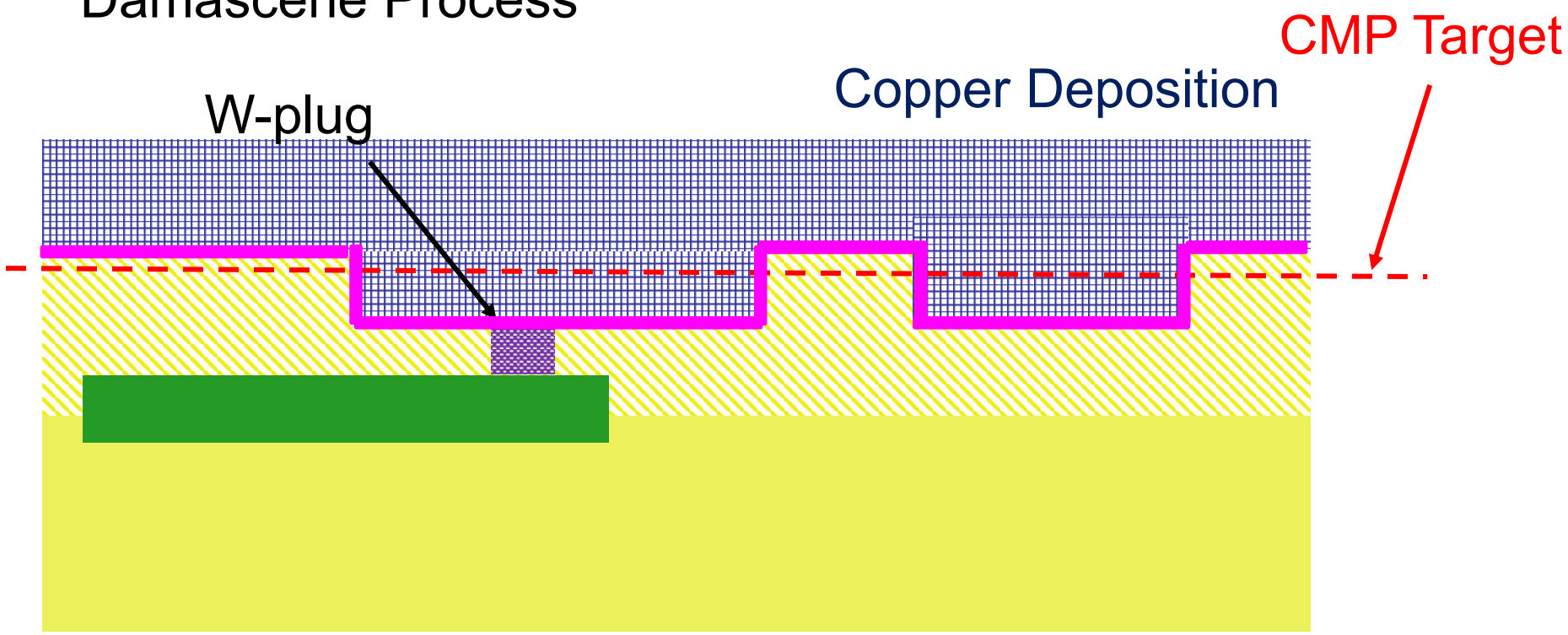
Damascene Process



Patterning of Copper

Consider Metal 1 (lowest level of metal)

Damascene Process



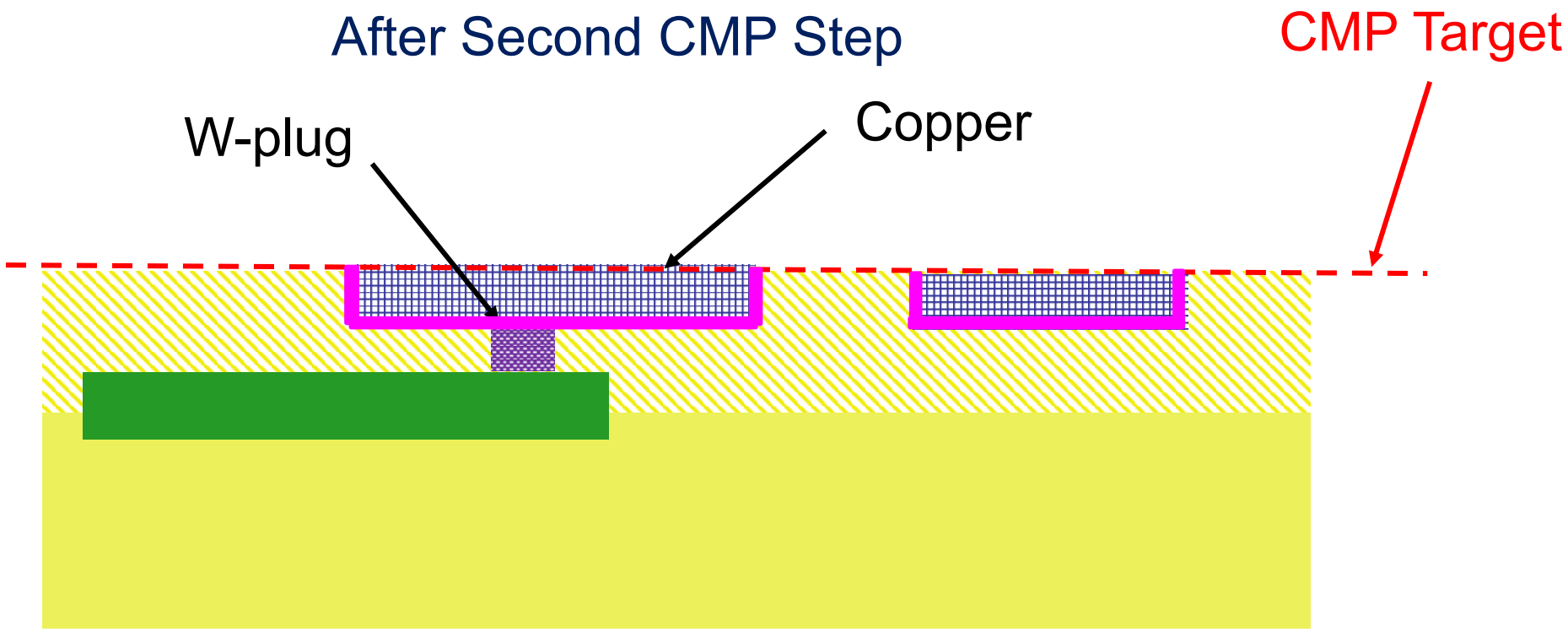
Copper is deposited or electroplated (Barrier Metal Used for Electroplating Seed)

Patterning of Copper

Consider Metal 1 (lowest level of metal)

Damascene Process

After Second CMP Step



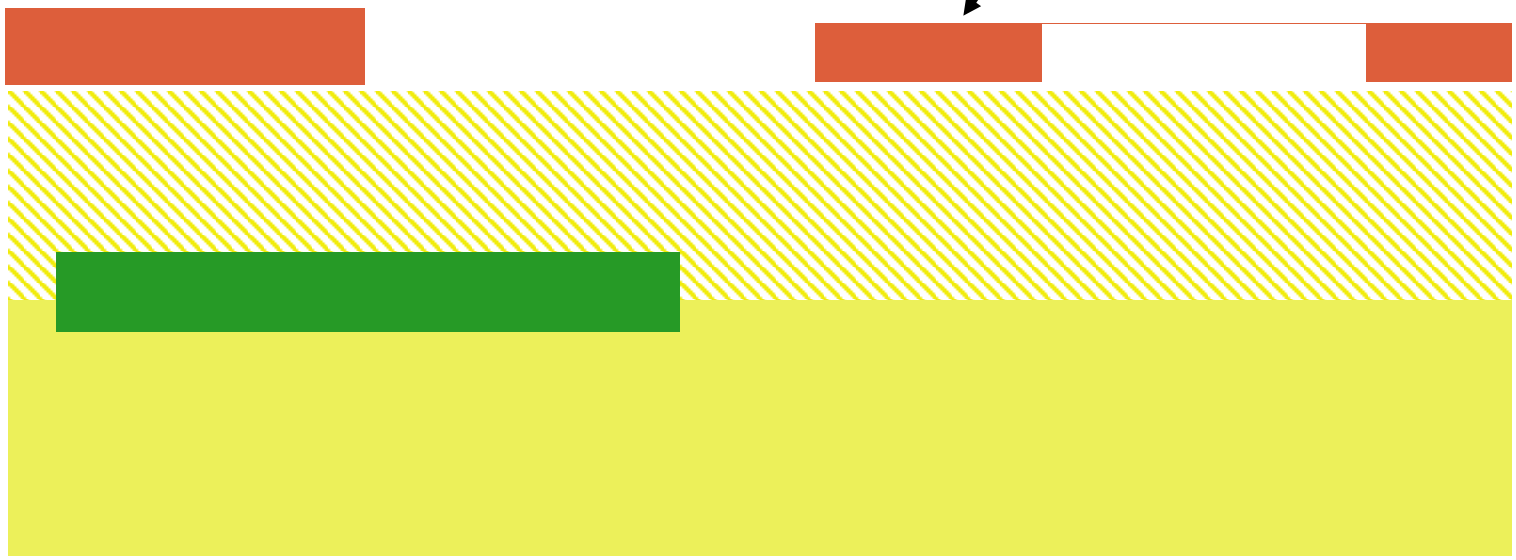
Patterning of Copper

Consider Metal 1 (lowest level of metal)

Dual-Damascene Process

Shallow Trench Defined in PR with Metal Mask

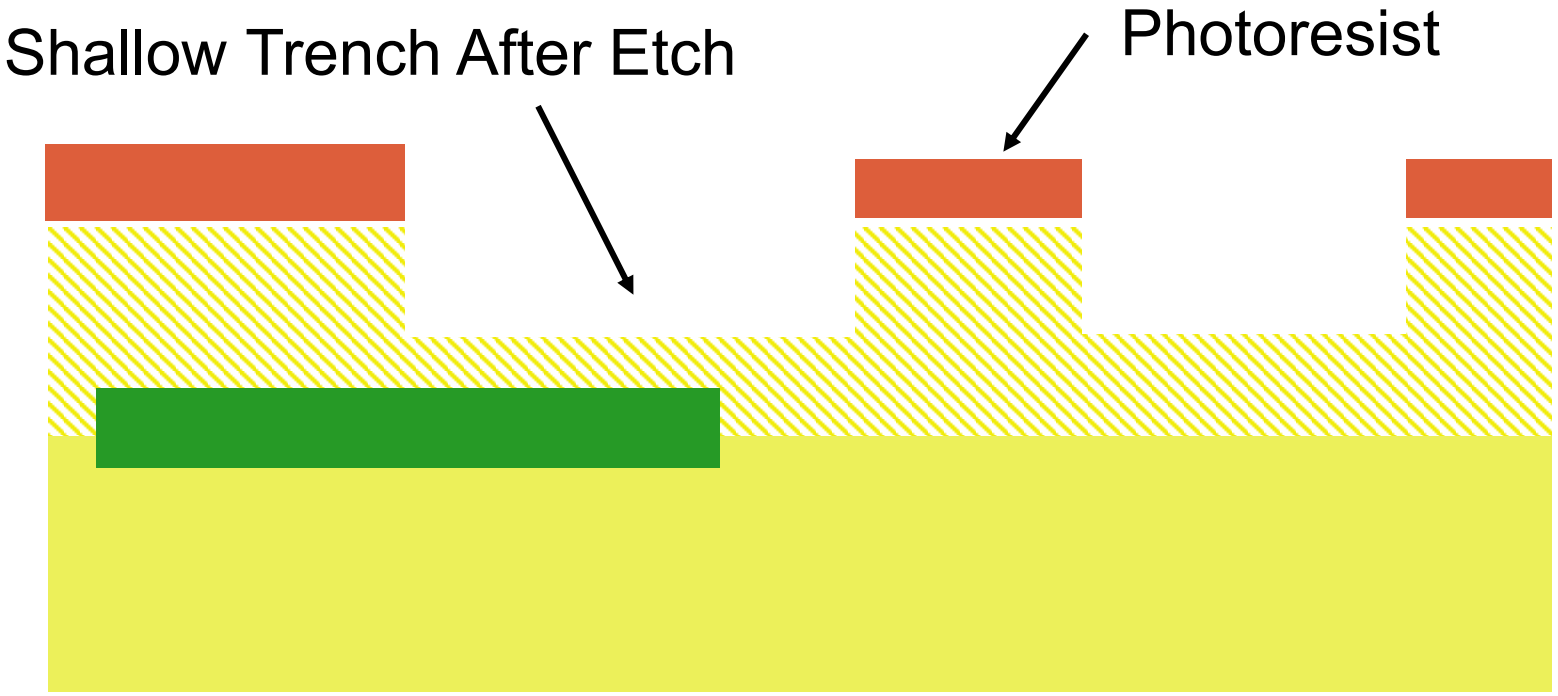
Photoresist



Patterning of Copper

Consider Metal 1 (lowest level of metal)

Dual-Damascene Process



Patterning of Copper

Consider Metal 1 (lowest level of metal)

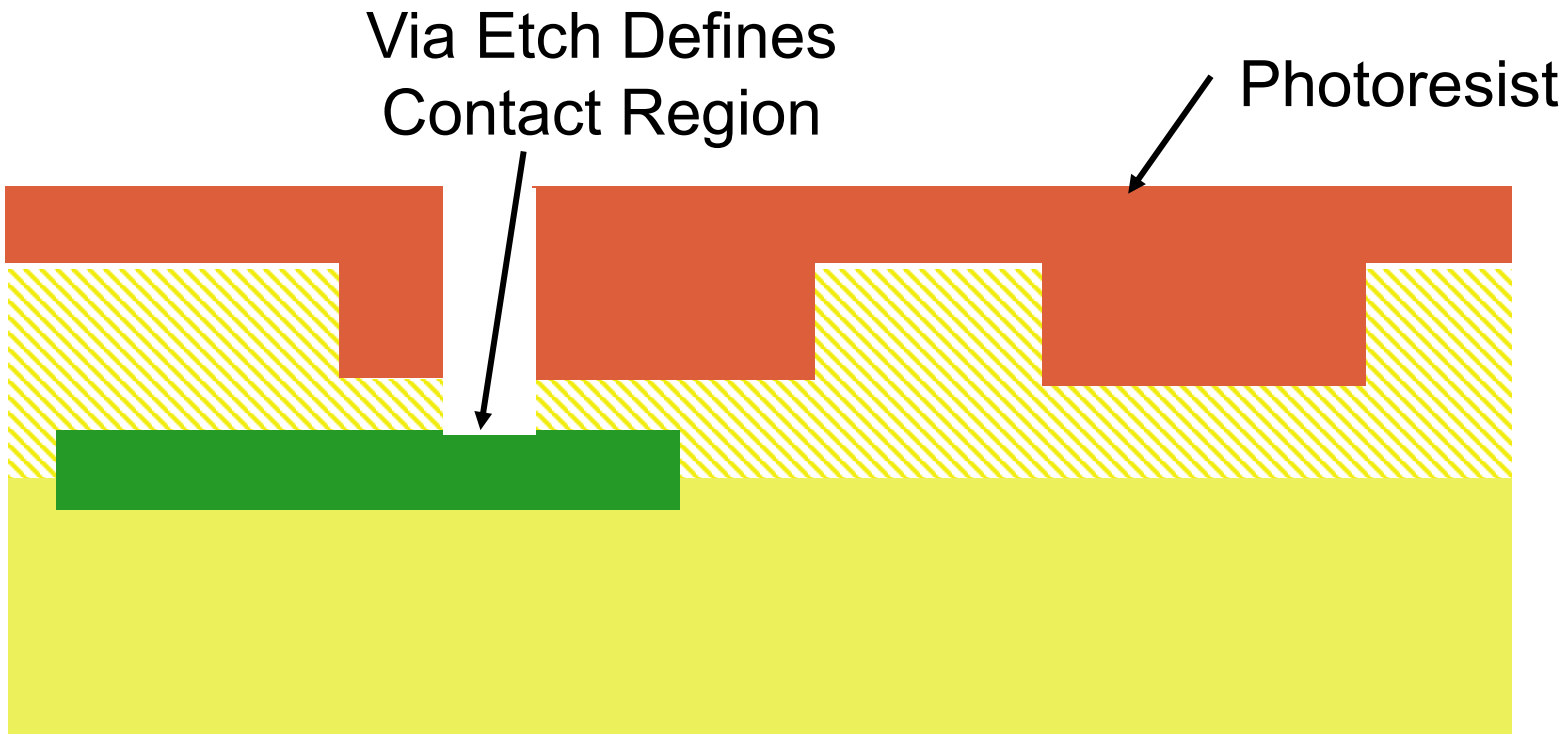
Dual-Damascene Process

Via Defined in PR
with Via Mask

Patterning of Copper

Consider Metal 1 (lowest level of metal)

Dual-Damascene Process



Patterning of Copper

Consider Metal 1 (lowest level of metal)

Dual-Damascene Process

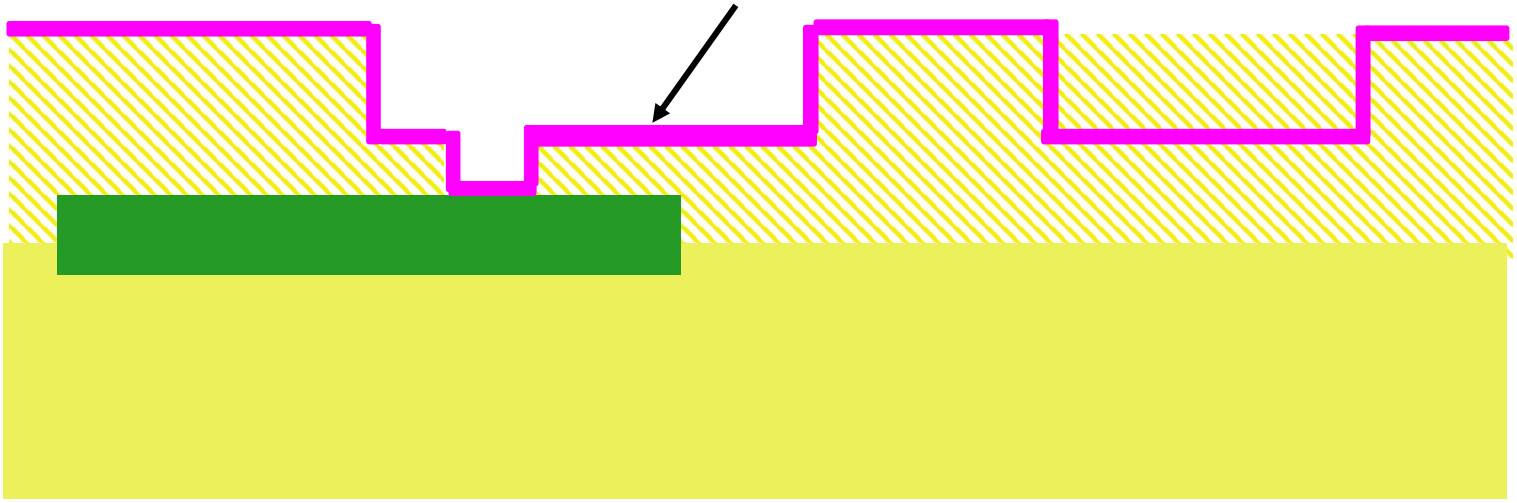
Via Etch Defines
Contact Region

Patterning of Copper

Consider Metal 1 (lowest level of metal)

Dual-Damascene Process

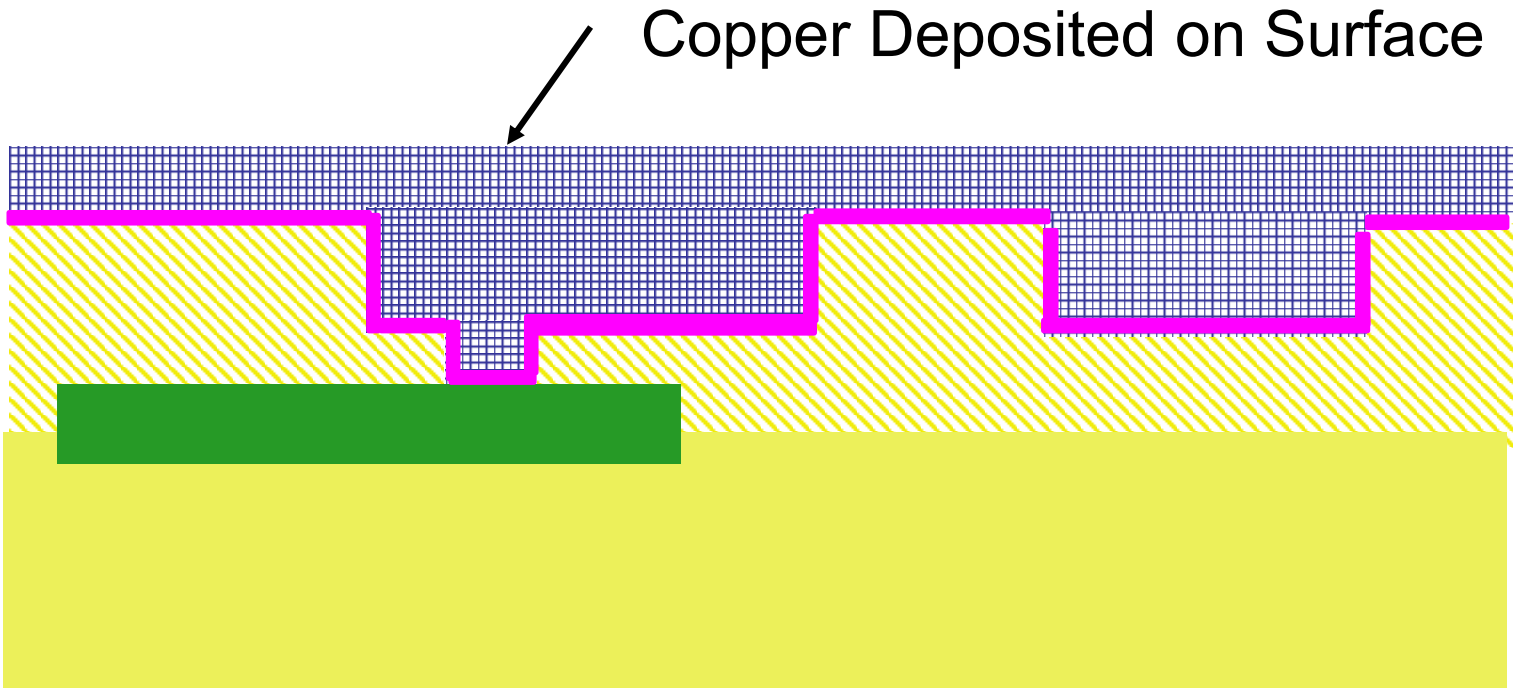
Barrier Metal (used for electroplating seed)



Patterning of Copper

Consider Metal 1 (lowest level of metal)

Dual-Damascene Process

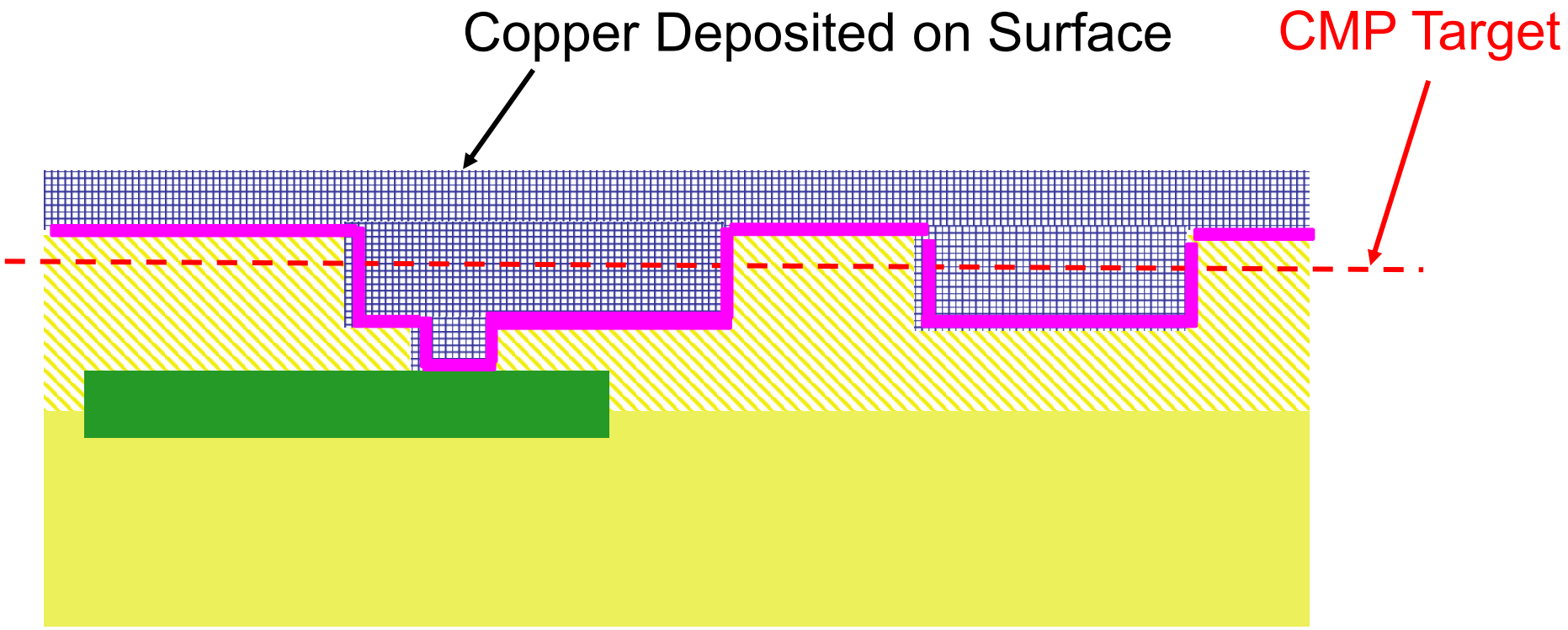


Copper is deposited or electroplated (Barrier Metal Used for Electroplating Seed)

Patterning of Copper

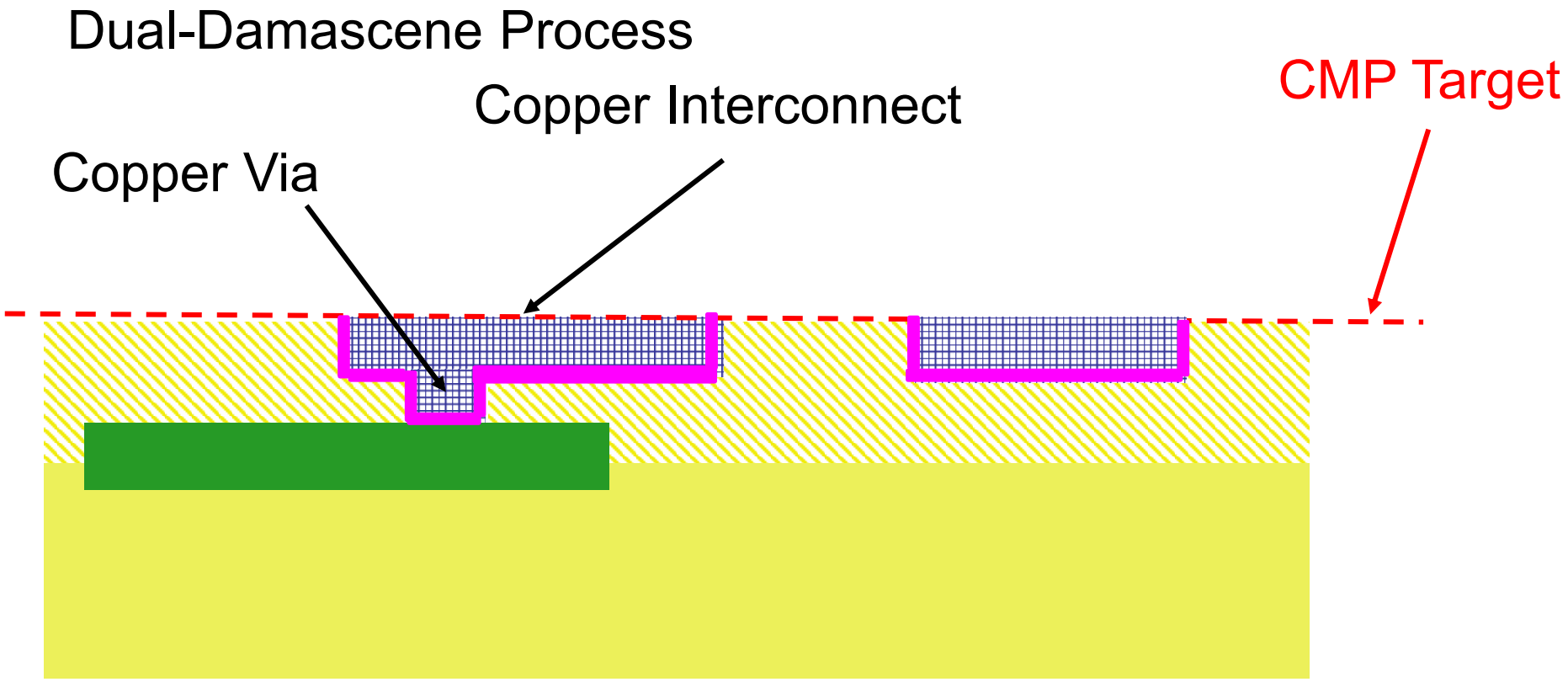
Consider Metal 1 (lowest level of metal)

Dual-Damascene Process

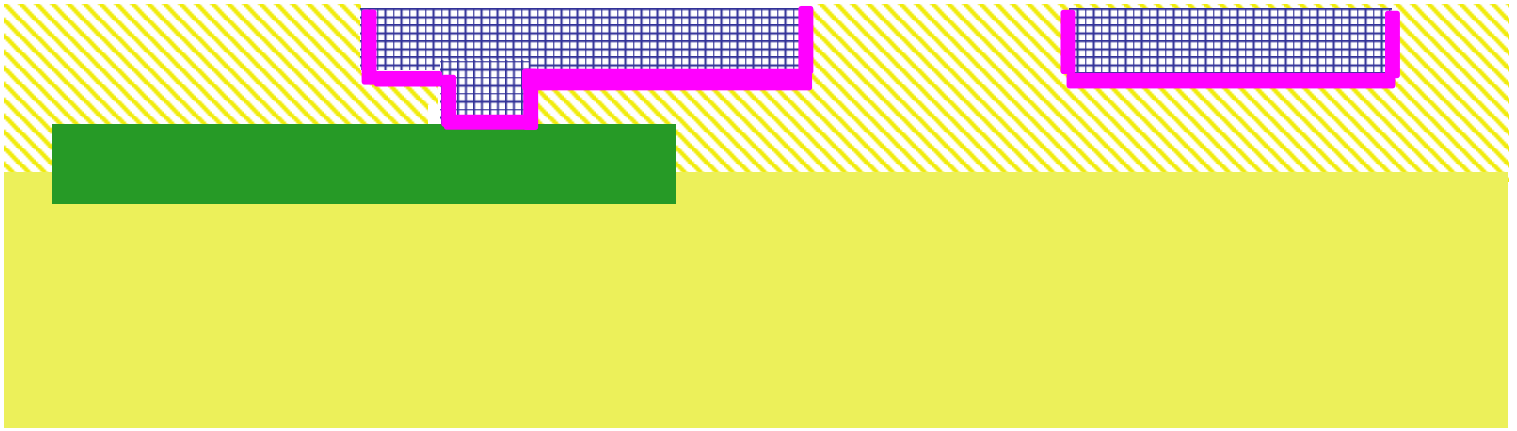


Patterning of Copper

Consider Metal 1 (lowest level of metal)



Patterning of Copper



Both Damascene Processes Realize Same Structure

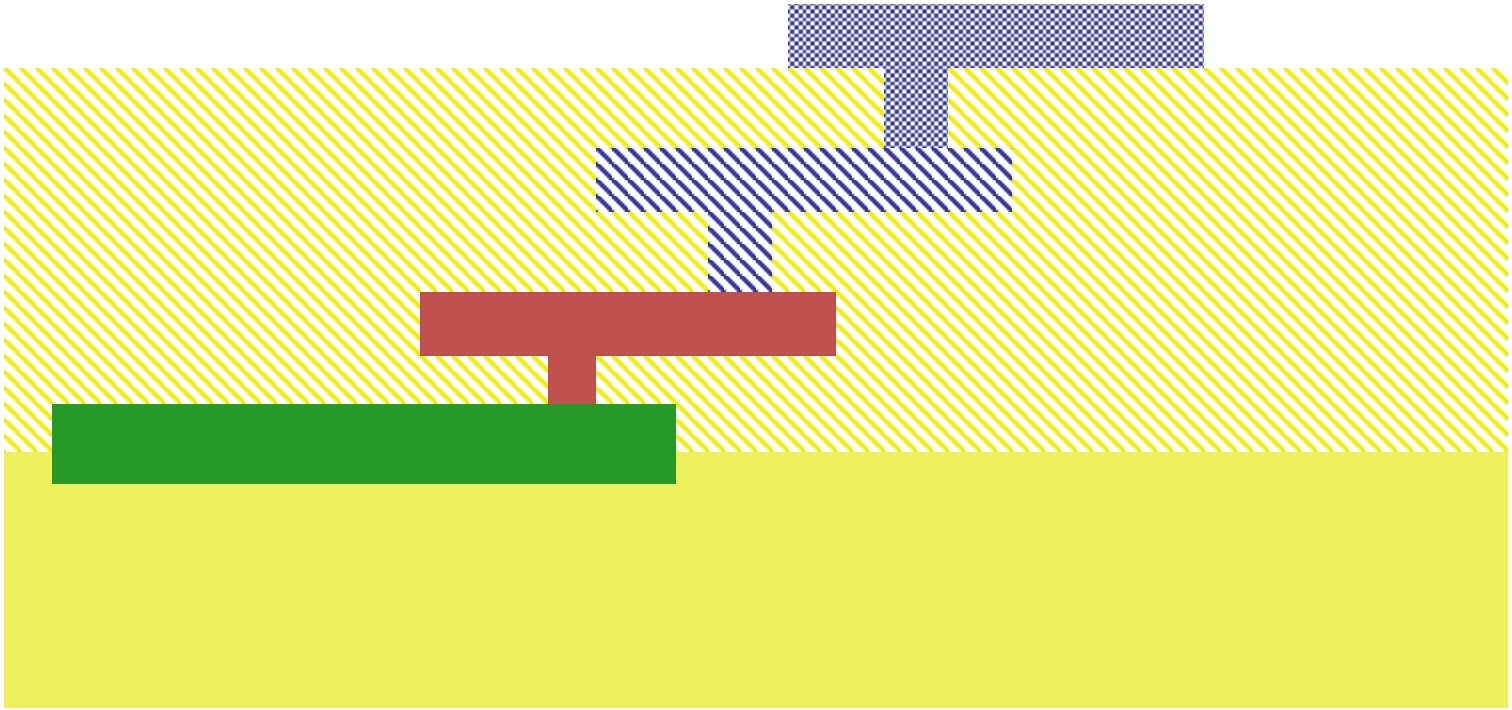
Damascene Process

Two Dielectric Deposition Steps
Two CMP Steps
Three Metal Deposition Steps
Two Dielectric Etches
W-Plug

Dual-Damascene Process

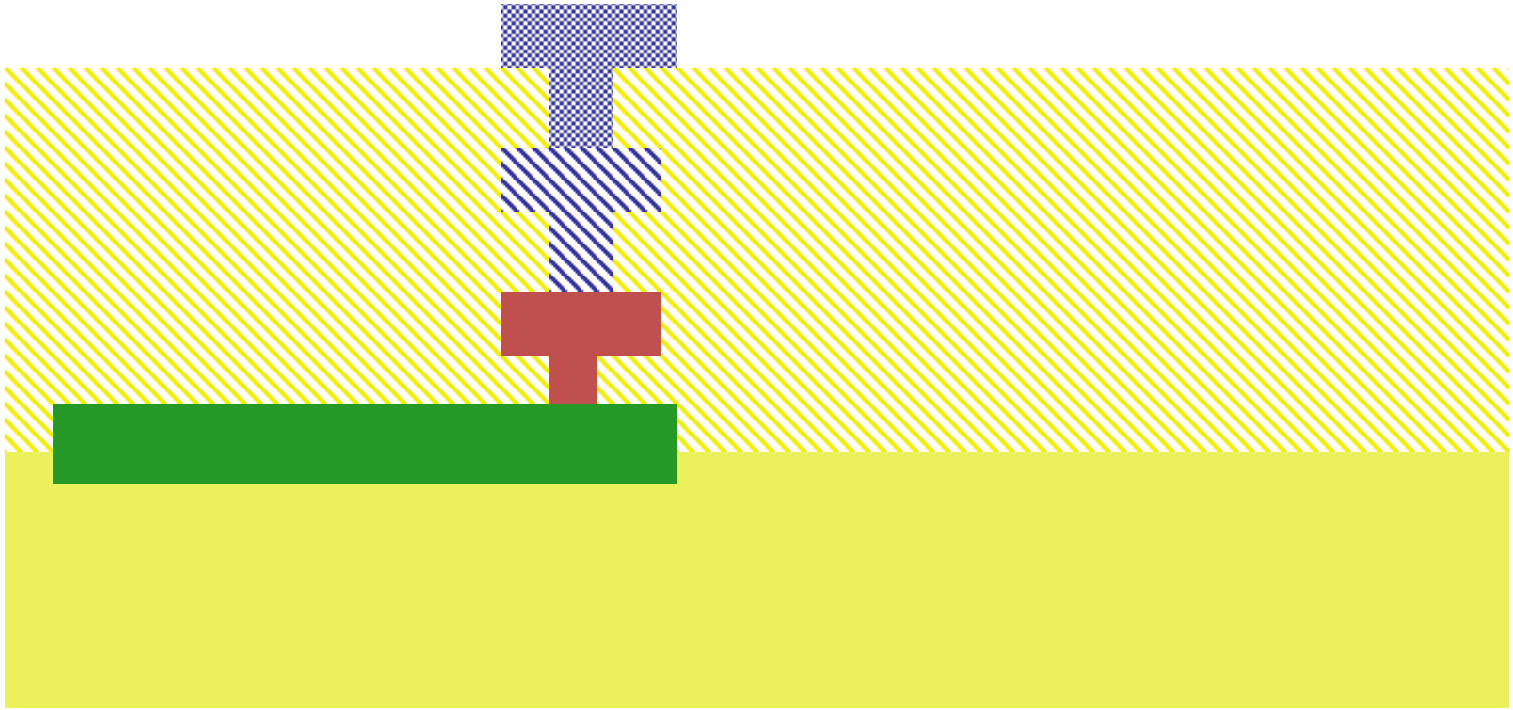
One Dielectric Deposition Step
Two CMP Steps
Two Metal Deposition Steps
Two Dielectric Etches
Via formed with metal step

Multiple Level Interconnects



3-rd level metal connection to n-active without stacked vias

Multiple Level Interconnects



3-rd level metal connection to n-active with stacked vias

Interconnect Layers May Vary in Thickness or Be Mostly Uniform

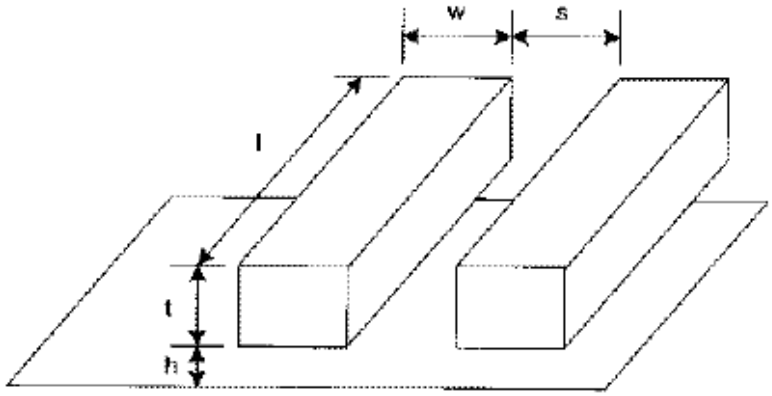


FIG 4.30 Interconnect geometry

Layer	t (nm)	w (nm)	s (nm)	AR
6	1720 1000	860	860	2.0
5	1600 1000	800	800	2.0
4	1080 700	540	540	2.0
3	700 700	320	320	2.2
2	700 700	320	320	2.2
1	480 800	250	250	1.9

Substrate

12.5μ

FIG 4.31 Layer stack for 6-metal Intel 180 nm process

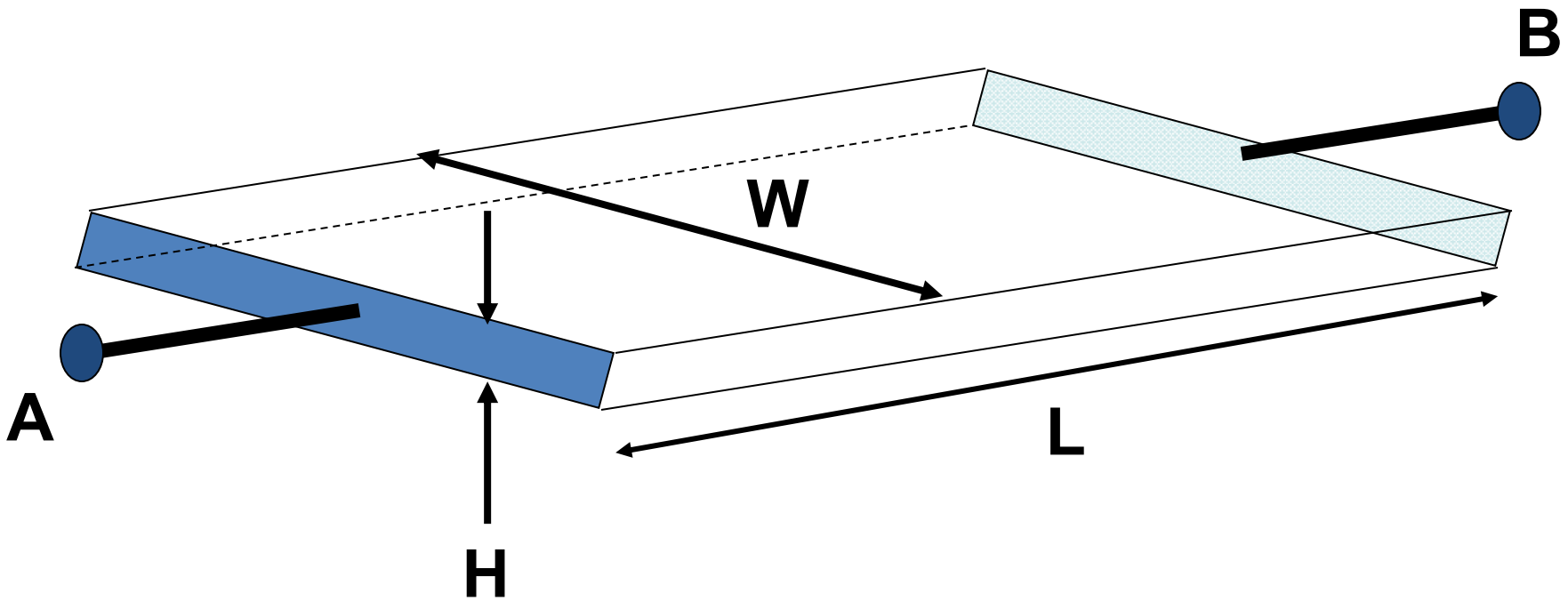
Interconnects

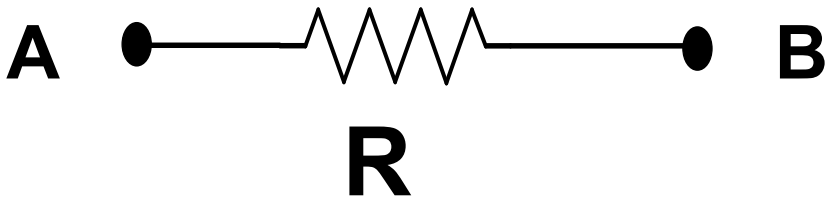
- Metal is preferred interconnect
  - Because conductivity is high
- Parasitic capacitances and resistances of concern in all interconnects
- Polysilicon used for short interconnects
  - Silicided to reduce resistance
  - Unsilicided when used as resistors
- Diffusion used for short interconnects
  - Parasitic capacitances are high

Interconnects

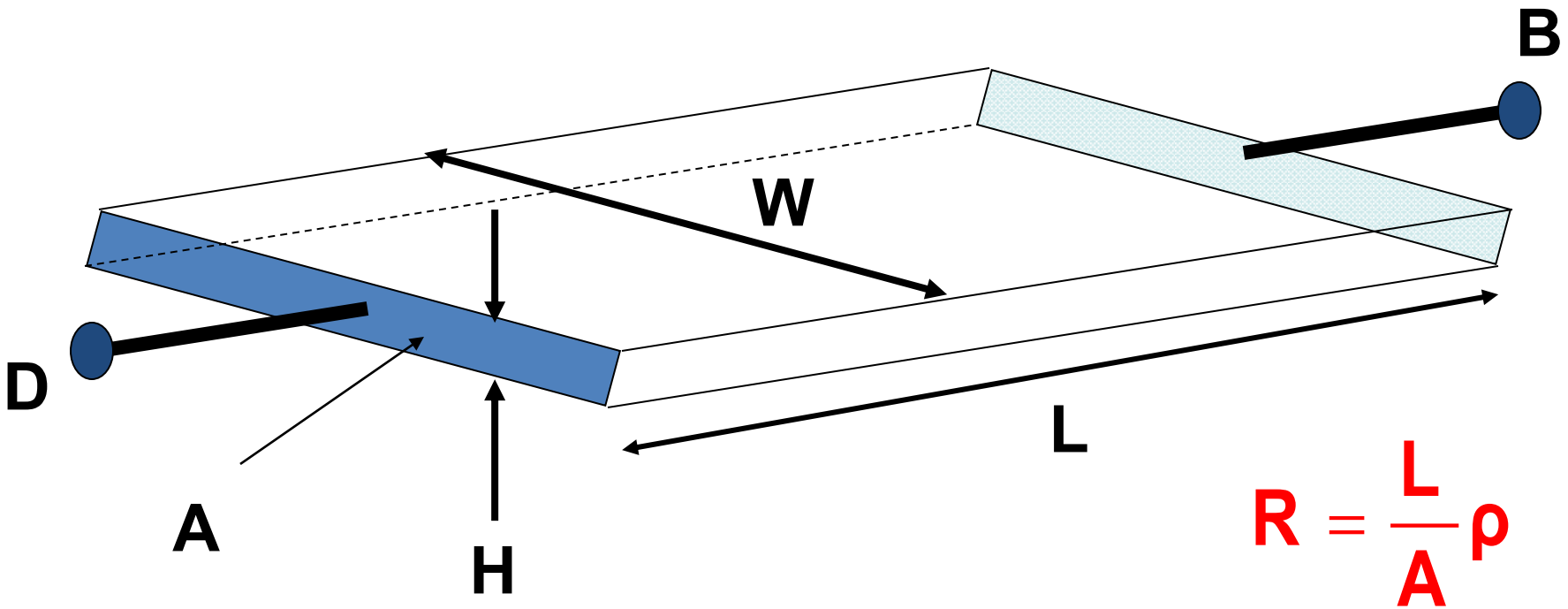
- Metal is preferred interconnect
  - Because conductivity is high
- Parasitic capacitances and resistances of concern in all interconnects
- Polysilicon used for short interconnects
  - Silicided to reduce resistance
  - Unsilicided when used as resistors
- Diffusion used for short interconnects
  - Parasitic capacitances are high

Resistance in Interconnects

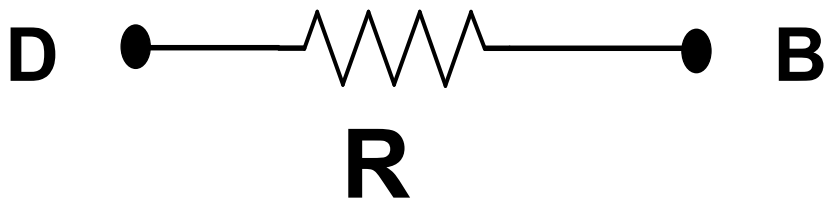




Resistance in Interconnects



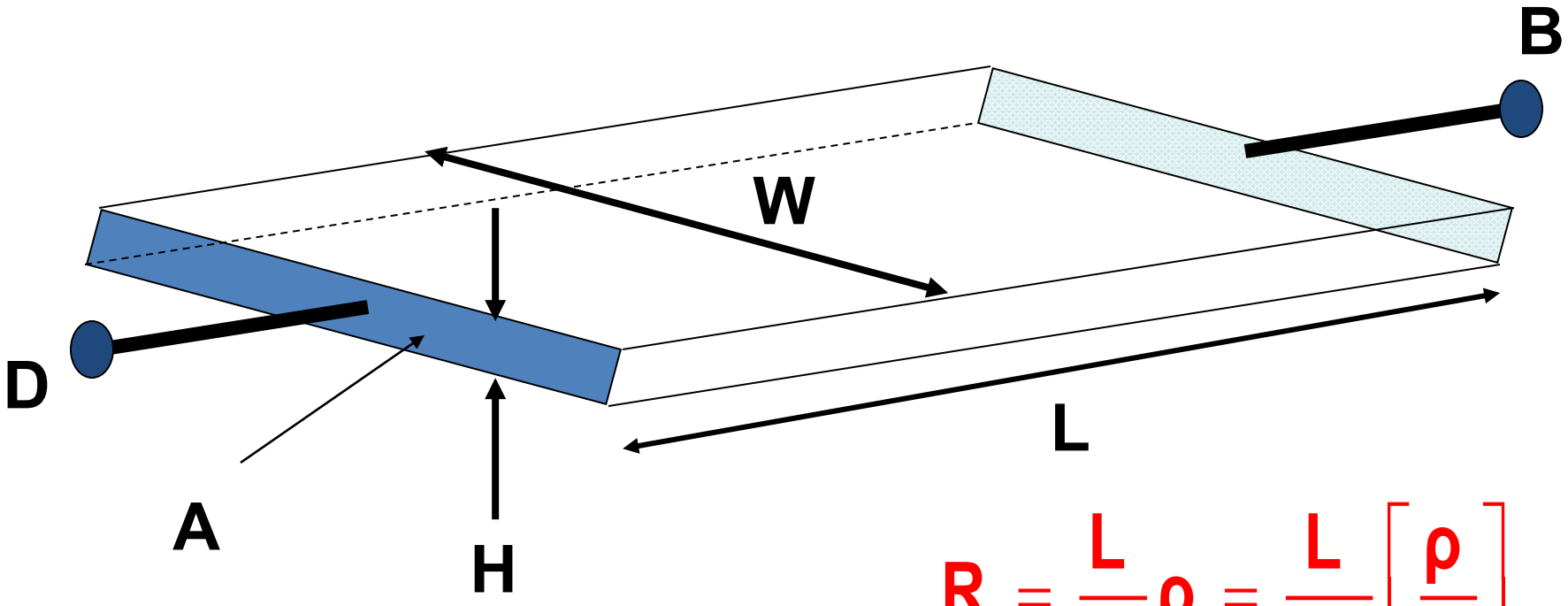
$$R = \frac{L}{A}\rho$$



A=HW

ρ independent of geometry and characteristic of the process

Resistance in Interconnects



$$R = \frac{L}{A}\rho = \frac{L}{W}\left[\frac{\rho}{H}\right]$$

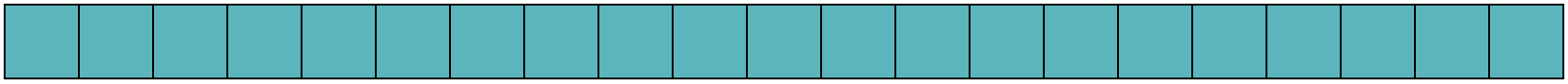
H << W and H << L in most processes
Interconnect behaves as a “thin” film
Sheet resistance often used instead of conductivity to characterize film

$R_{\square}=\rho/H$ $R=R_{\square}[L / W]$

Resistance in Interconnects

$$R = R_{\square}[L / W]$$

The “Number of Squares” approach to resistance determination in thin films

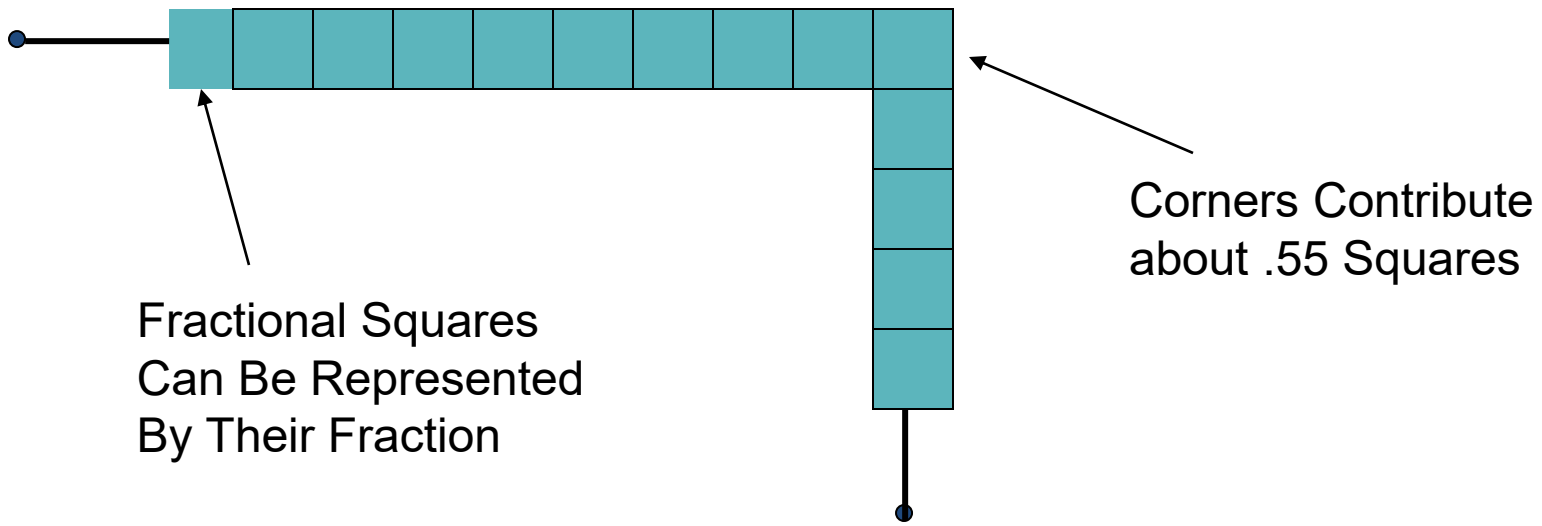


$N_S = 21$

$L / W = 21$

$$R = R_{\square} N_S$$

Resistance in Interconnects



The “squares” approach is not exact but is good enough for calculating resistance in almost all applications

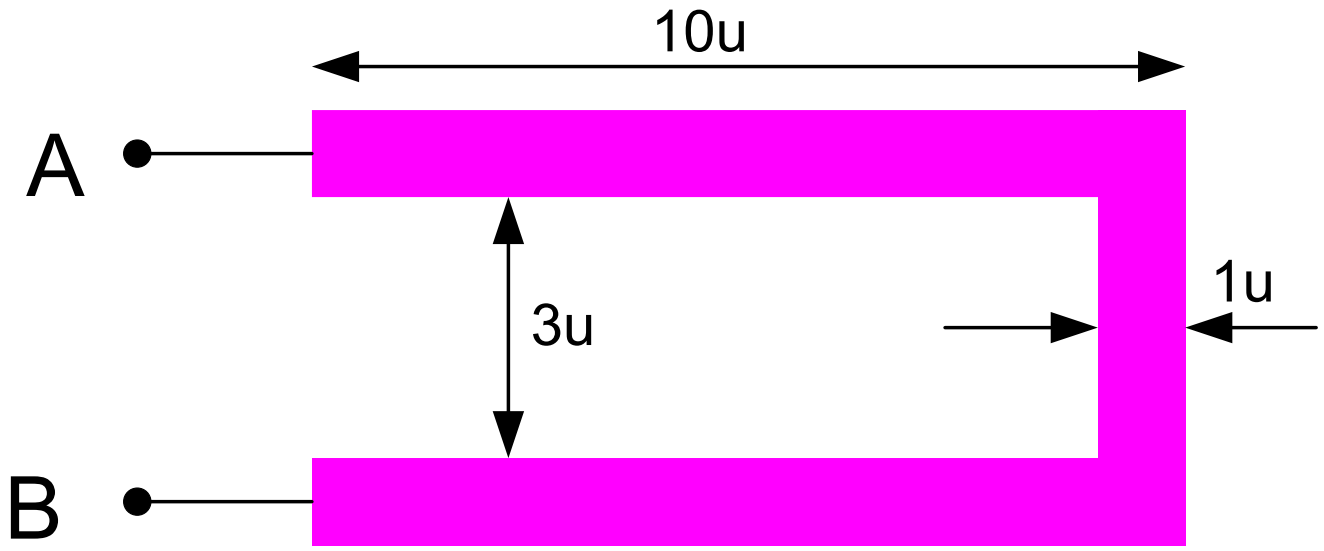
In this example:

$$N_S = 12 + .55 + .7 = 13.25$$

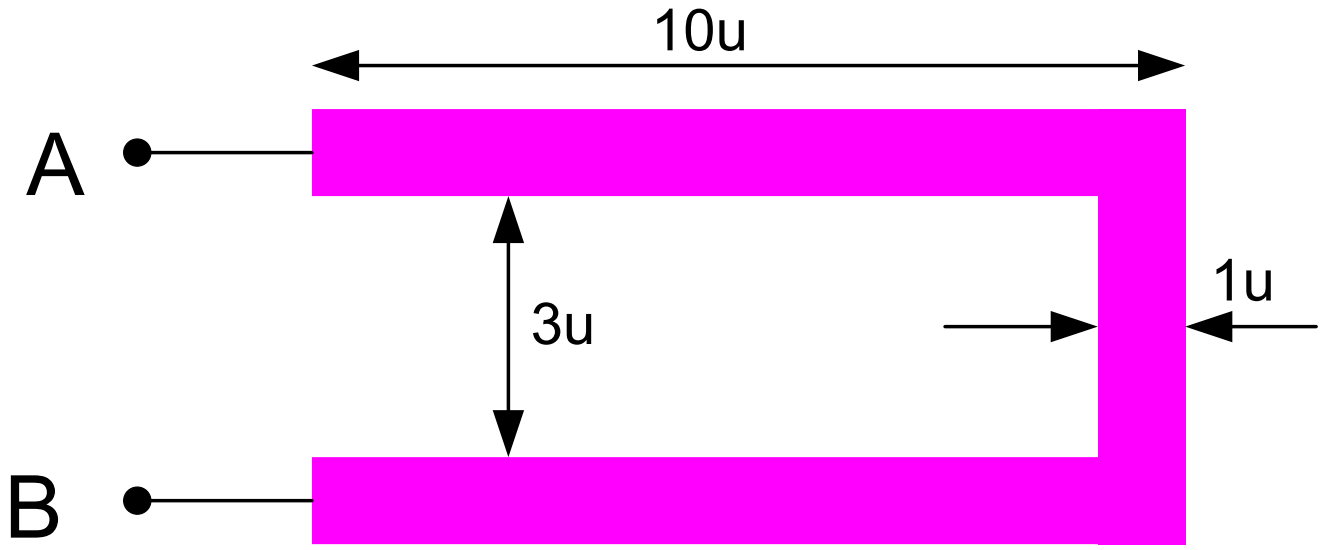
$$\mathbf{R = R_{\square} 13.25}$$

Example:

The layout of a film resistor with electrodes A and B is shown. If the sheet resistance of the film is 40 Ω/□, determine the resistance between nodes A and B.



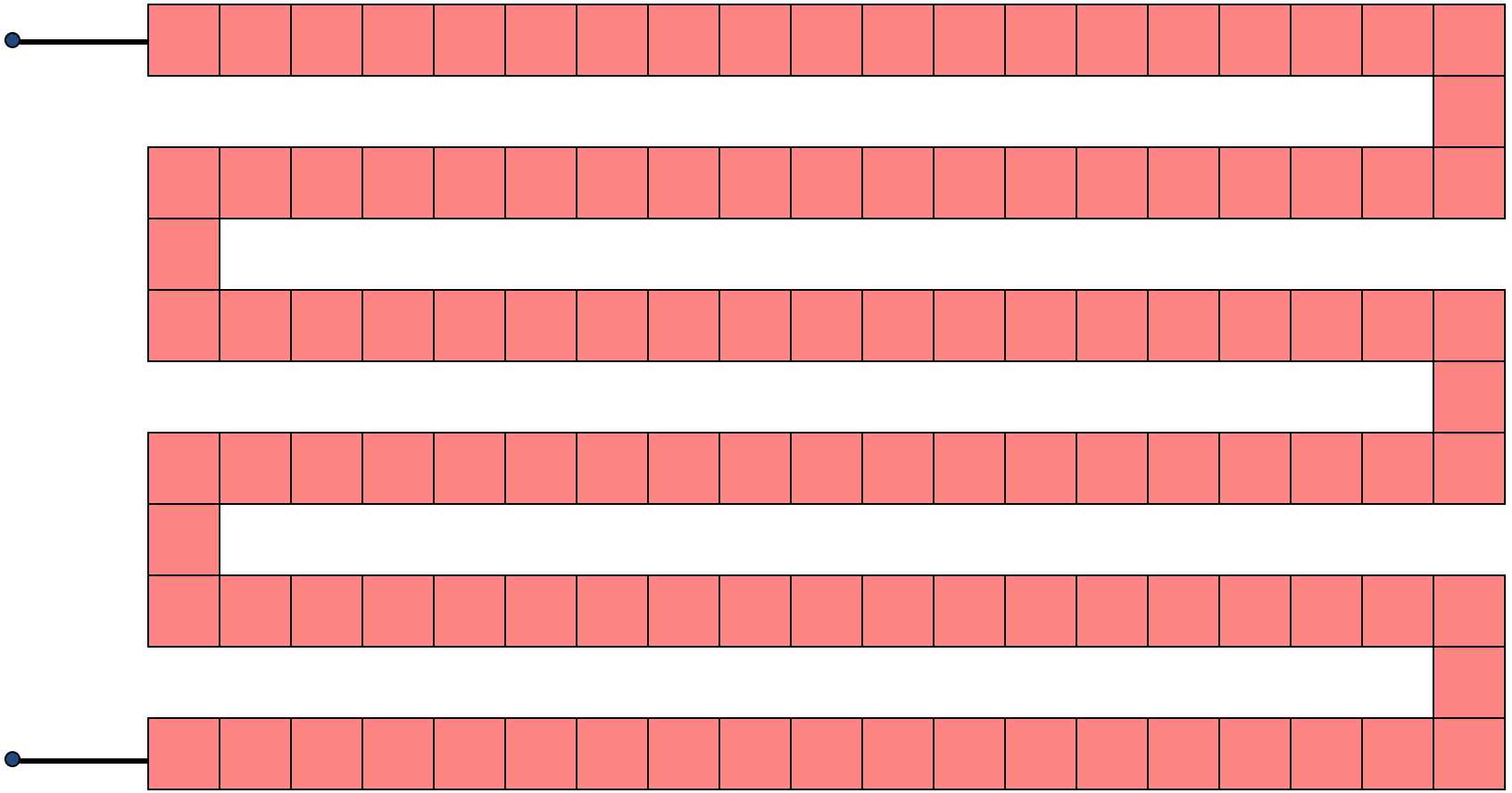
Solution



$N_S = 9+9+3+2(.55)=22.1$

$R_{AB}=R_{\square}N_S=40x22.1=884\Omega$

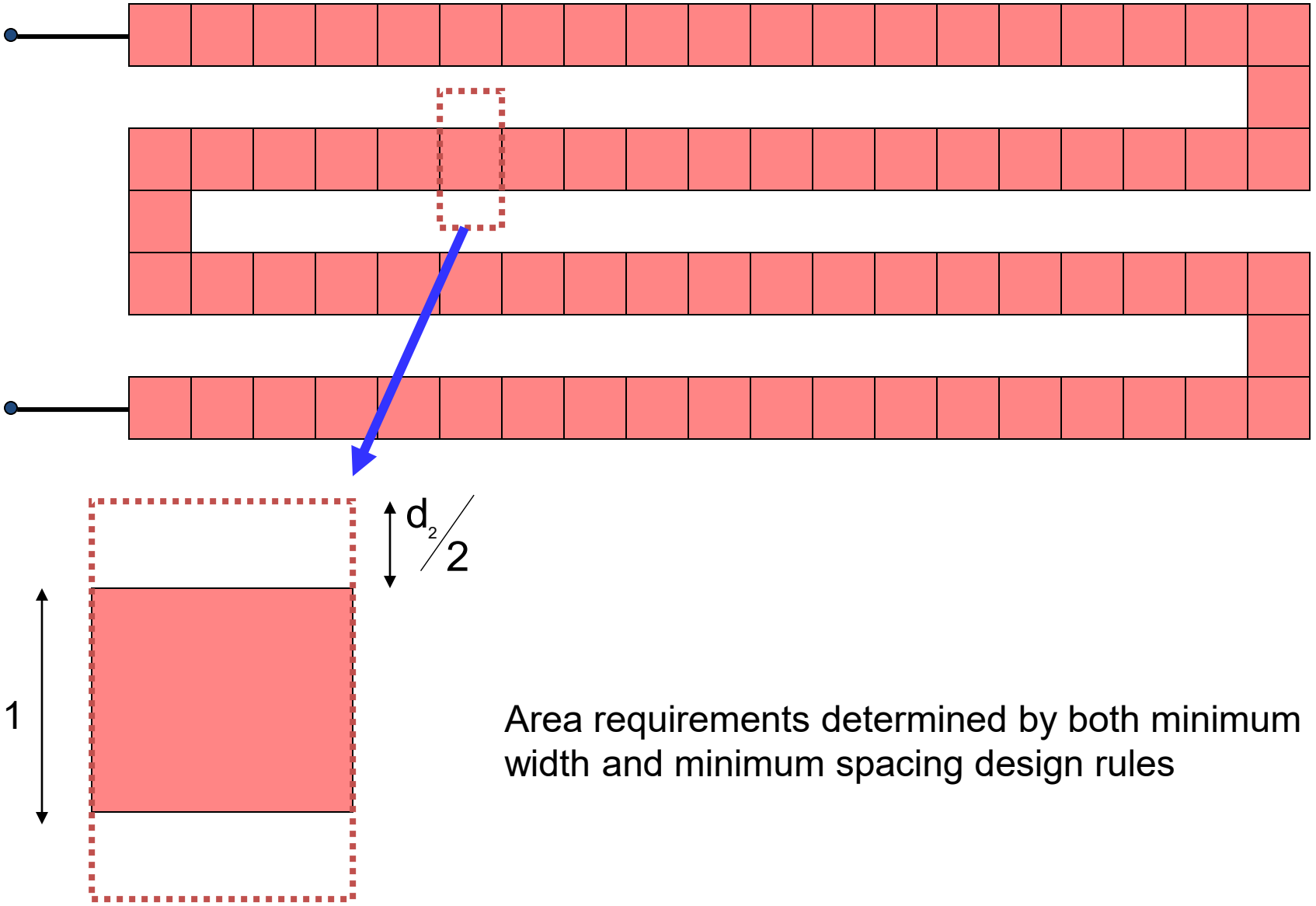
Resistance in Interconnects
(can be used to build resistors!)



- Serpentine often used when large resistance required
- Polysilicon or diffusion often used for resistor creation
- Effective at managing the aspect ratio of large resistors
- May include hundreds or even thousands of squares

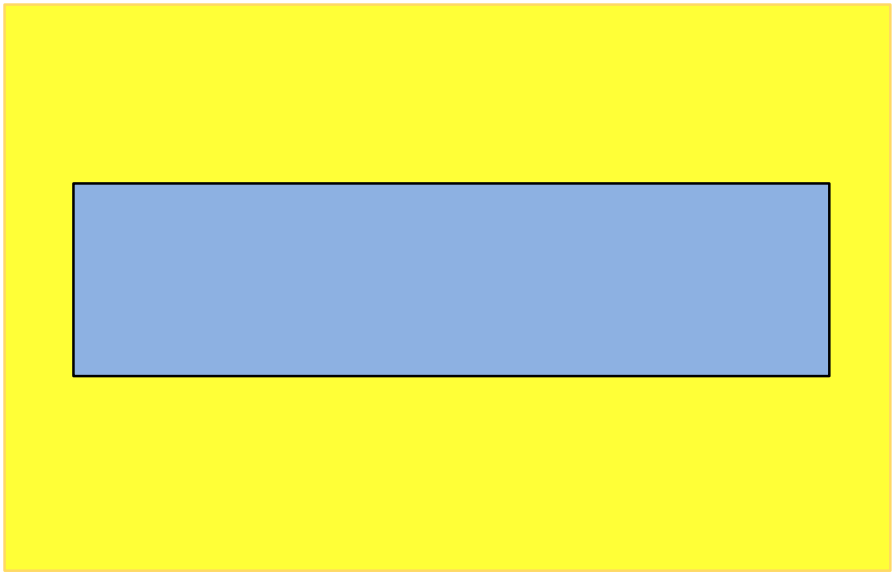
Resistance in Interconnects

(can be used to build resistors!)



Area requirements determined by both minimum width and minimum spacing design rules

Capacitance in Interconnects

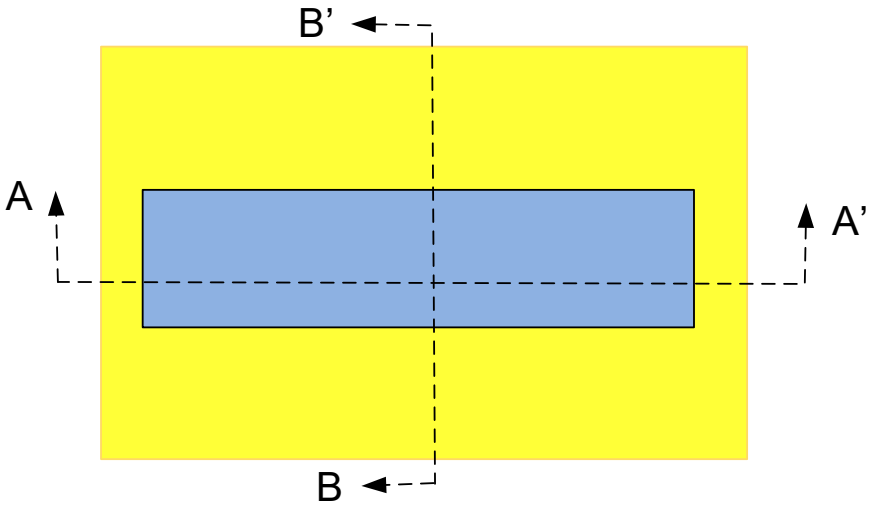


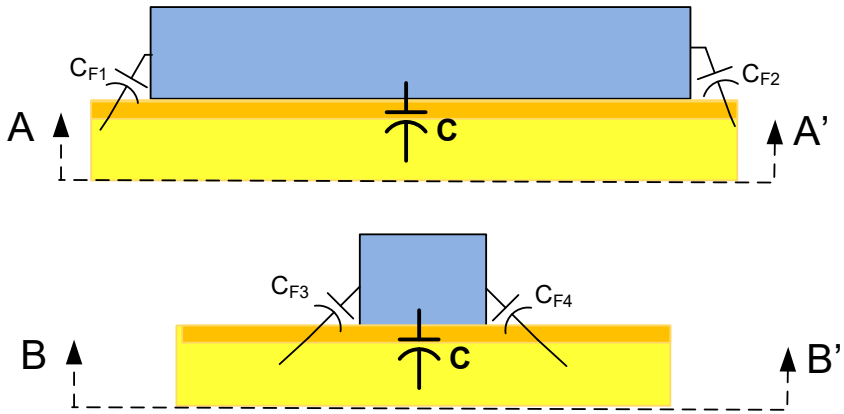
$$C=C_D A$$

C_D is the capacitance density and A is the area of the overlap

(actually there is also a small fringe capacitance that has been neglected)

Capacitance in Interconnects



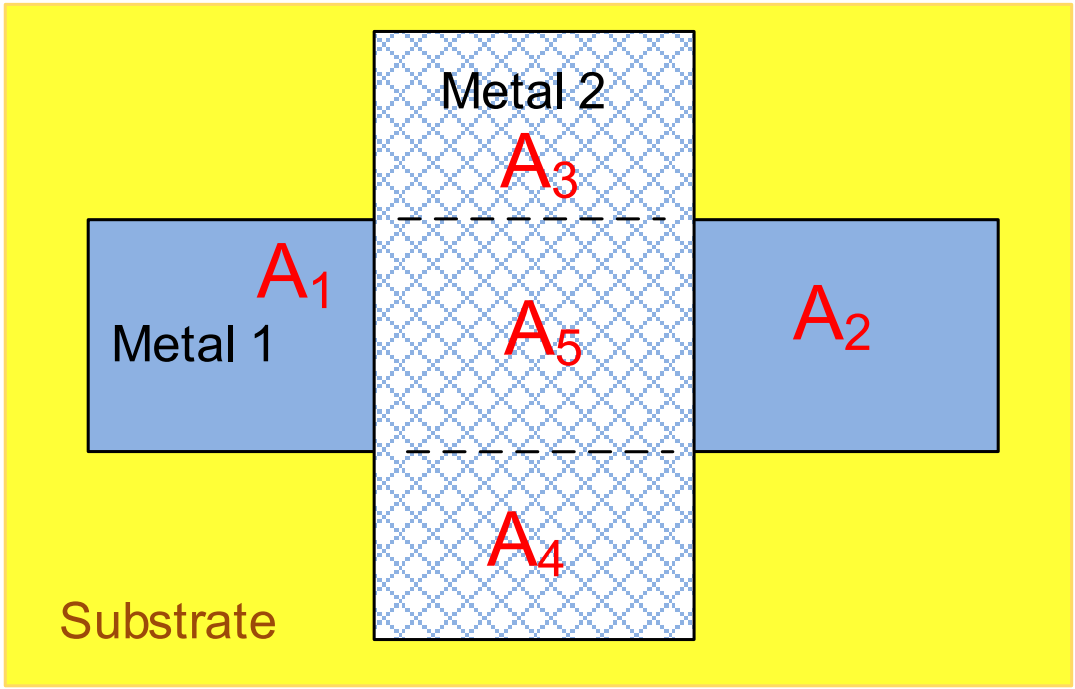


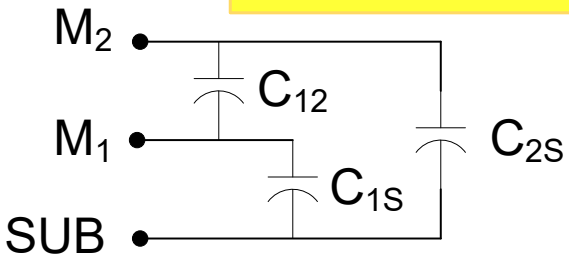
$$C=C_DA$$

fringe capacitances denoted by C_{F1},C_{F2},C_{F3} and C_{F4}

$C_F = C_{F1}+C_{F2}+C_{F3}+C_{F2}$ is usually small compared to C

Capacitance in Interconnects





$$C_{12}=CD_{12}\,A_5$$

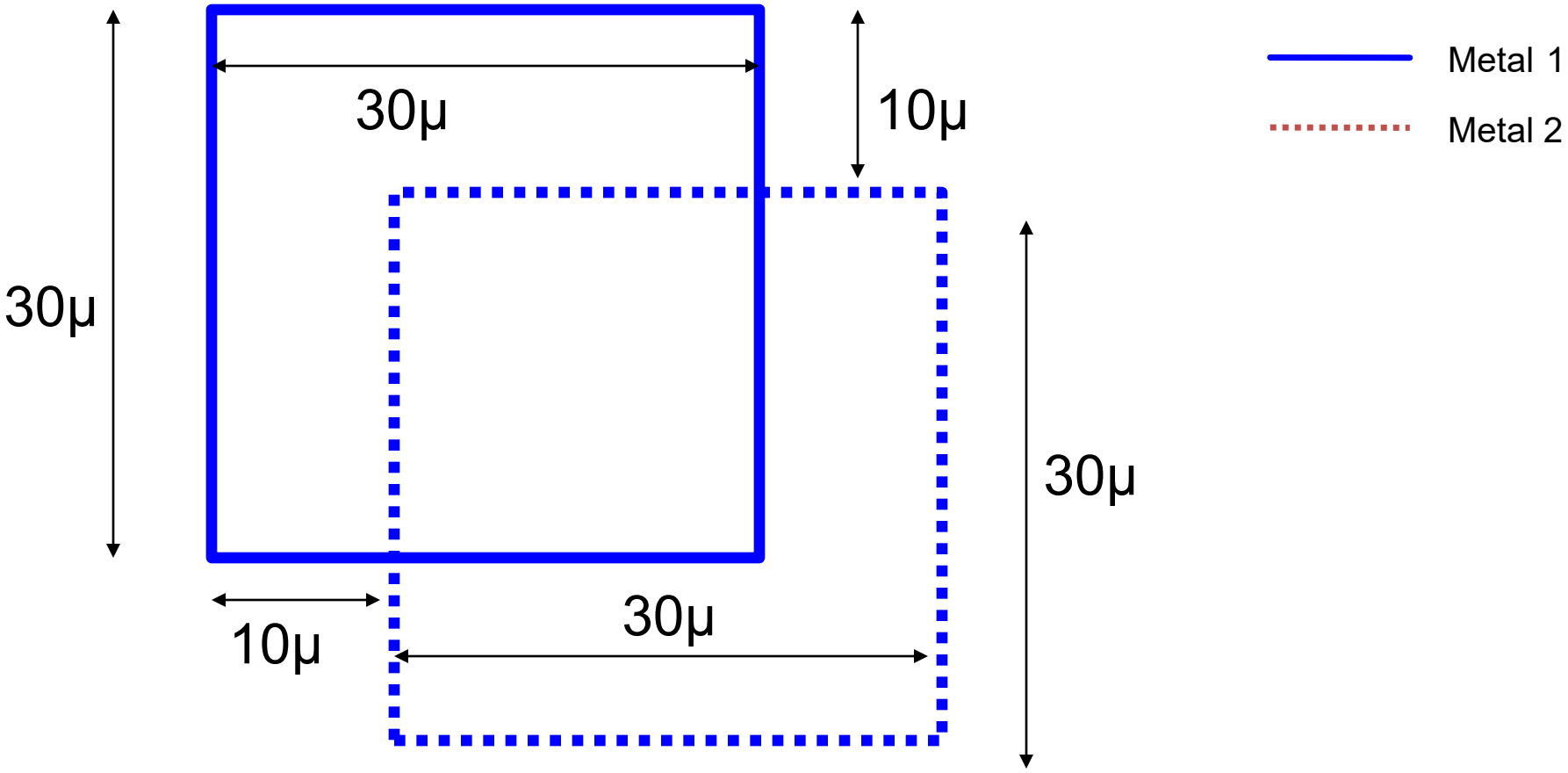
$$C_{1S}=CD_{1S}\,(A_1+A_2+A_5)$$

$$C_{2S}=CD_{2S}\,(A_3+A_4)$$

Equivalent Circuit

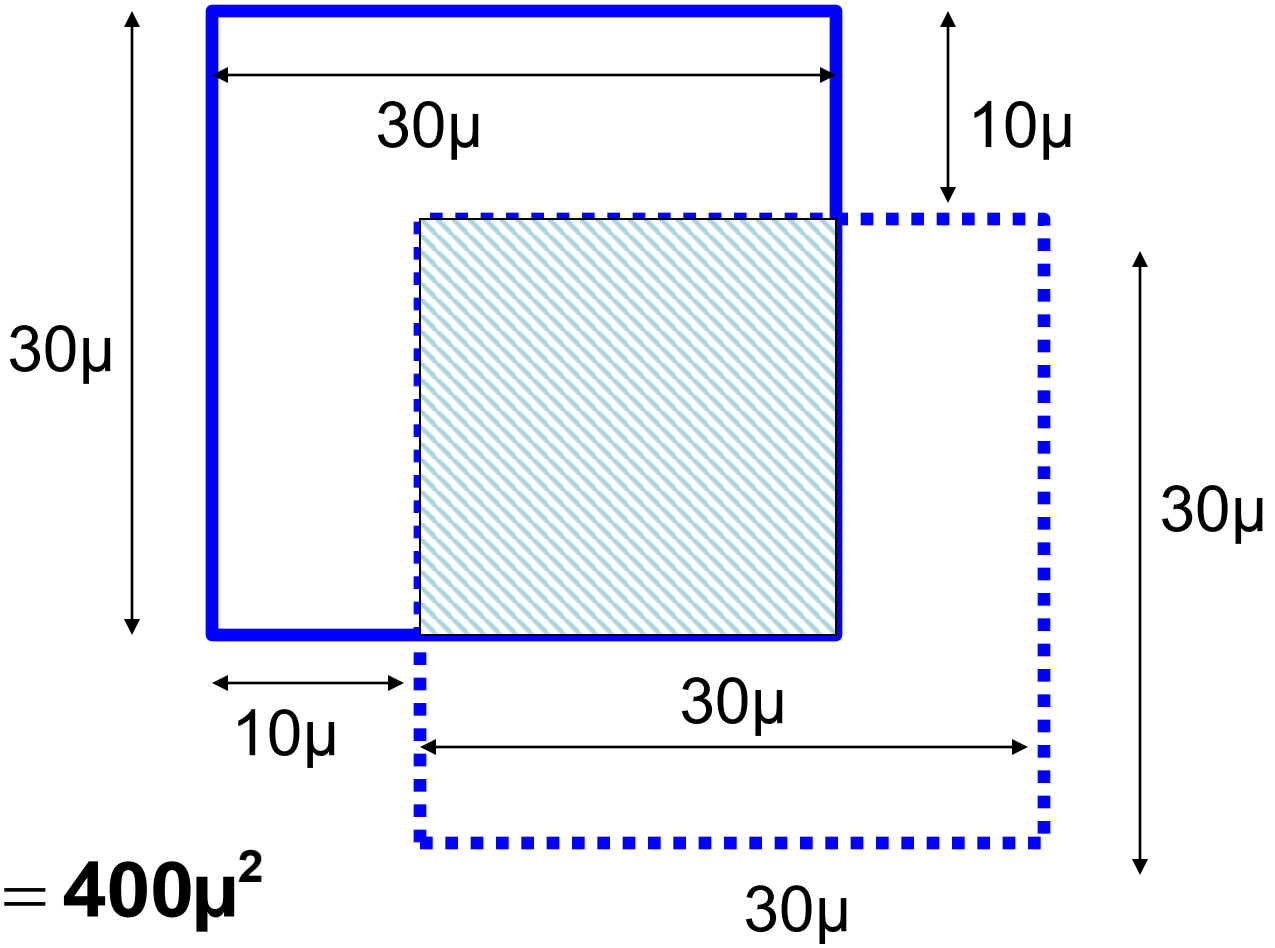
Example

Two metal layers, Metal 1 and Metal 2, are shown. Both are above field oxide. Determine the capacitance between Metal 1 and Metal 2. Assume the process has capacitance densities from M_1 to substrate of .05fF/u^2, from M_1 to M_2 of .07fF/u^2 and from M_2 to substrate of .025fF/u^2.



Example

Solution



$$A_{C1C2} = (20\mu)^2 = 400\mu^2$$

The capacitance density from M_1 to M_2 is .07fF/u^2

$$C_{12} = A_{C1C2} \bullet C_{D12} = 400\mu^2 \bullet 0.07\text{fF}/\mu^2 = 28\text{fF}$$

Capacitance and Resistance in Interconnects

- See MOSIS WEB site for process parameters that characterize parasitic resistances and capacitances

www.mosis.org

MOSIS WAFER ACCEPTANCE TESTS

RUN: T6AU
TECHNOLOGY: SCN05

VENDOR: AMIS
FEATURE SIZE: 0.5 microns

Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		446	-239	uA/um
Vth		0.68	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.9	-11.6	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.48	0.58	V^0.5
K' (Uo*Cox/2)		56.4	-18.2	uA/V^2
Low-field Mobility		463.87	149.69	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
---	---	---

SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.5	105.3	23.5	999	44.2	0.09	0.10	ohms/sq
Contact Resistance	64.9	149.7	17.3		29.2		0.97	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	824	816	ohms/sq
Contact Resistance	0.79			ohms

COMMENTS: N\POLY is N-well under polysilicon.

Note: substrate for p+ is the n-well

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	aF/um^2
Area (N+active)			2434		35	16	11		aF/um^2
Area (P+active)			2335						aF/um^2
Area (poly)				938	56	15	9		aF/um^2
Area (poly2)					49				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							35		aF/um^2
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts

Voh (100 uA)	2.0	4.85	volts
Vinv	2.0	2.46	volts
Gain	2.0	-19.72	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		95.31	MHz
D256_WIDE (31-stg,5.0V)		147.94	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.49	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		1.01	uW/MHz/gate

COMMENTS: SUBMICRON

□ T6AU SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

```
* DATE: Jan 11/07
* LOT: T6AU                    WAF: 7101
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 1.42E-8
+XJ      = 1.5E-7         NCH     = 1.7E17         VTH0    = 0.629035
+K1      = 0.8976376      K2      = -0.09255       K3      = 24.0984767
+K3B     = -8.2369696     W0      = 1.041146E-8    NLX     = 1E-9
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 2.7123969      DVT1    = 0.4232931      DVT2    = -0.1403765
+U0      = 451.2322004    UA      = 3.091785E-13   UB      = 1.702517E-18
+UC      = 1.22401E-11    VSAT    = 1.715884E5     A0      = 0.6580918
+AGS     = 0.130484       B0      = 2.446405E-6    B1      = 5E-6
+KETA    = -3.043349E-3   A1      = 8.18159E-7     A2      = 0.3363058
+RDSW    = 1.367055E3     PRWG    = 0.0328586      PRWB    = 0.0104806
+WR      = 1              WINT    = 2.443677E-7    LINT    = 6.999776E-8
+XL      = 1E-7           XW      = 0              DWG     = -1.256454E-8
+DWB     = 3.676235E-8    VOFF    = -1.493503E-4   NFACTOR = 1.0354201
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 2.342963E-3    ETAB    = -1.5324E-4
+DSUB    = 0.0764123      PCLM    = 2.5941582      PDIBLC1 = 0.8187825
+PDIBLC2 = 2.366707E-3    PDIBLCB = -0.0431505     DROUT   = 0.9919348
+PSCBE1  = 6.611774E8     PSCBE2  = 3.238266E-4    PVAG    = 0
+DELTA   = 0.01           RSH     = 83.5           MOBMOD  = 1
```

```
+PRT      = 0              UTE      = -1.5           KT1      = -0.11
+KT1L     = 0              KT2      = 0.022          UA1      = 4.31E-9
+UB1      = -7.61E-18      UC1      = -5.6E-11       AT       = 3.3E4
+WL       = 0              WLN      = 1              WW       = 0
+WWN      = 1              WWL      = 0              LL       = 0
+LLN      = 1              LW       = 0              LWN      = 1
+LWL      = 0              CAPMOD   = 2              XPART    = 0.5
+CGDO     = 2.32E-10       CGSO     = 2.32E-10       CGBO     = 1E-9
+CJ       = 4.282017E-4    PB       = 0.9317787      MJ       = 0.4495867
+CJSW     = 3.034055E-10   PBSW     = 0.8            MJSW     = 0.1713852
+CJSWG    = 1.64E-10       PBSWG    = 0.8            MJSWG    = 0.1713852
+CF       = 0              PVTH0    = 0.0520855      PRDSW    = 112.8875816
+PK2      = -0.0289036     WKETA    = -0.0237483     LKETA    = 1.728324E-3     )
*
.MODEL CMOSP PMOS (                                  LEVEL    = 49
+VERSION = 3.1             TNOM     = 27             TOX      = 1.42E-8
+XJ       = 1.5E-7         NCH      = 1.7E17         VTH0     = -0.9232867
+K1       = 0.5464347      K2       = 8.119291E-3    K3       = 5.1623206
+K3B      = -0.8373484     W0       = 1.30945E-8     NLX      = 5.772187E-8
+DVT0W    = 0              DVT1W    = 0              DVT2W    = 0
+DVT0     = 2.0973823      DVT1     = 0.5356454      DVT2     = -0.1185455
+U0       = 220.5922586    UA       = 3.144939E-9    UB       = 1E-21
+UC       = -6.19354E-11   VSAT     = 1.176415E5     A0       = 0.8441929
+AGS      = 0.1447245      B0       = 1.149181E-6    B1       = 5E-6
+KETA     = -1.093365E-3   A1       = 3.467482E-4    A2       = 0.4667486
+RDSW     = 3E3            PRWG     = -0.0418549     PRWB     = -0.0212201
+WR       = 1              WINT     = 3.007497E-7    LINT     = 1.040439E-7
+XL       = 1E-7           XW       = 0              DWG      = -2.133809E-8
+DWB      = 1.706031E-8    VOFF     = -0.0801591     NFACTOR  = 0.9468597
+CIT      = 0              CDSC     = 2.4E-4         CDSCD    = 0
+CDSCB    = 0              ETA0     = 0.4060383      ETAB     = -0.0633609
+DSUB     = 1              PCLM     = 2.2703293      PDIBLC1  = 0.0279014
+PDIBLC2  = 3.201161E-3    PDIBLCB  = -0.057478      DROUT    = 0.1718548
+PSCBE1   = 4.876974E9     PSCBE2   = 5E-10          PVAG     = 0
+DELTA    = 0.01           RSH      = 105.3          MOBMOD   = 1
+PRT      = 0              UTE      = -1.5           KT1      = -0.11
+KT1L     = 0              KT2      = 0.022          UA1      = 4.31E-9
+UB1      = -7.61E-18      UC1      = -5.6E-11       AT       = 3.3E4
+WL       = 0              WLN      = 1              WW       = 0
+WWN      = 1              WWL      = 0              LL       = 0
+LLN      = 1              LW       = 0              LWN      = 1
+LWL      = 0              CAPMOD   = 2              XPART    = 0.5
+CGDO     = 3.12E-10       CGSO     = 3.12E-10       CGBO     = 1E-9
```

```
+CJ       = 7.254264E-4     PB       = 0.9682229       MJ       = 0.4969013
+CJSW     = 2.496599E-10    PBSW     = 0.99            MJSW     = 0.386204
+CJSWG    = 6.4E-11         PBSWG    = 0.99            MJSWG    = 0.386204
+CF       = 0               PVTH0    = 5.98016E-3      PRDSW    = 14.8598424
+PK2      = 3.73981E-3      WKETA    = 7.286716E-4     LKETA    = -4.768569E-3    )
*
```

MOSIS WAFER ACCEPTANCE TESTS

RUN: T4BK (MM_NON-EPI_THK-MTL)
TECHNOLOGY: SCN018

VENDOR: TSMC
FEATURE SIZE: 0.18 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.53	volts
SHORT	20.0/0.18			
Idss		571	-266	uA/um
Vth		0.51	-0.53	volts
Vpt		4.7	-5.5	volts
WIDE	20.0/0.18			
Ids0		22.0	-5.6	pA/um
LARGE	50/50			
Vth		0.42	-0.41	volts
Vjbkd		3.1	-4.1	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		171.8	-36.3	uA/V^2
Low-field Mobility		398.02	84.10	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>6.6	<-6.6	volts

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

Note: substrate for p+ is the n-well

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

T4BK SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jan 21/05
* LOT: T4BK WAF: 3004

```
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1           TNOM    = 27              TOX     = 4E-9
+XJ      = 1E-7          NCH     = 2.3549E17       VTH0    = 0.3662648
+K1      = 0.5802748     K2      = 3.124029E-3     K3      = 1E-3
+K3B     = 3.3886871     W0      = 1E-7            NLX     = 1.766159E-7
+DVT0W   = 0             DVT1W   = 0               DVT2W   = 0
+DVT0    = 1.2312416     DVT1    = 0.3849841       DVT2    = 0.0161351
+U0      = 265.1889031   UA      = -1.506402E-9    UB      = 2.489393E-18
+UC      = 5.621884E-11  VSAT    = 1.017932E5      A0      = 2
+AGS     = 0.4543117     B0      = 3.433489E-7     B1      = 5E-6
+KETA    = -0.0127714    A1      = 1.158074E-3     A2      = 1
+RDSW    = 136.5582806   PRWG    = 0.5             PRWB    = -0.2
+WR      = 1             WINT    = 0               LINT    = 1.702415E-8
+XL      = 0             XW      = -1E-8           DWG     = -4.211574E-9
+DWB     = 1.107719E-8   VOFF    = -0.0948017      NFACTOR = 2.1860065
+CIT     = 0             CDSC    = 2.4E-4          CDSCD   = 0
+CDSCB   = 0             ETA0    = 3.335516E-3     ETAB    = 6.028975E-5
+DSUB    = 0.0214781     PCLM    = 0.6602119       PDIBLC1 = 0.1605325
+PDIBLC2 = 3.287142E-3   PDIBLCB = -0.1            DROUT   = 0.7917811
+PSCBE1  = 6.420235E9    PSCBE2  = 4.122516E-9     PVAG    = 0.0347169
+DELTA   = 0.01          RSH     = 6.6             MOBMOD  = 1
+PRT     = 0             UTE     = -1.5            KT1     = -0.11
+KT1L    = 0             KT2     = 0.022           UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11        AT      = 3.3E4
+WL      = 0             WLN     = 1               WW      = 0
+WWN     = 1             WWL     = 0               LL      = 0
+LLN     = 1             LW      = 0               LWN     = 1
+LWL     = 0             CAPMOD  = 2               XPART   = 0.5
+CGDO    = 8.06E-10      CGSO    = 8.06E-10        CGBO    = 1E-12
+CJ      = 9.895609E-4   PB      = 0.8             MJ      = 0.3736889
+CJSW    = 2.393608E-10  PBSW    = 0.8             MJSW    = 0.1537892
+CJSWG   = 3.3E-10       PBSWG   = 0.8             MJSWG   = 0.1537892
+CF      = 0             PVTH0   = -1.73163E-3     PRDSW   = -1.4173554
+PK2     = 1.600729E-3   WKETA   = 1.601517E-3     LKETA   = -3.255127E-3
+PU0     = 5.2024473     PUA     = 1.584315E-12    PUB     = 7.446142E-25
+PVSAT   = 1.686297E3    PETA0   = 1.001594E-4     PKETA   = -2.039532E-3    )
*
```

```
.MODEL CMOSP PMOS (                                LEVEL   = 49
+VERSION = 3.1          TNOM    = 27               TOX     = 4E-9
+XJ      = 1E-7         NCH     = 4.1589E17        VTH0    = -0.3708038
+K1      = 0.5895473    K2      = 0.0235946        K3      = 0
+K3B     = 13.8642028   W0      = 1E-6             NLX     = 1.517201E-7
+DVT0W   = 0            DVT1W   = 0                DVT2W   = 0
+DVT0    = 0.7885088    DVT1    = 0.2564577        DVT2    = 0.1
+U0      = 103.0478426  UA      = 1.049312E-9      UB      = 2.545758E-21
+UC      = -1E-10       VSAT    = 1.645114E5       A0      = 1.627879
+AGS     = 0.3295499    B0      = 5.207699E-7      B1      = 1.370868E-6
+KETA    = 0.0296157    A1      = 0.4449009        A2      = 0.3
+RDSW    = 306.5789827  PRWG    = 0.5              PRWB    = 0.5
+WR      = 1            WINT    = 0                LINT    = 2.761033E-8
+XL      = 0            XW      = -1E-8            DWG     = -2.433889E-8
+DWB     = -9.34648E-11 VOFF    = -0.0867009       NFACTOR = 2
+CIT     = 0            CDSC    = 2.4E-4           CDSCD   = 0
+CDSCB   = 0            ETA0    = 1.018318E-3      ETAB    = -3.206319E-4
+DSUB    = 1.094521E-3  PCLM    = 1.3281073        PDIBLC1 = 2.394169E-3
+PDIBLC2 = -3.255915E-6 PDIBLCB = -1E-3            DROUT   = 0
+PSCBE1  = 4.881933E10  PSCBE2  = 5E-10            PVAG    = 2.0932623

+DELTA   = 0.01         RSH     = 7.5              MOBMOD  = 1
+PRT     = 0            UTE     = -1.5             KT1     = -0.11
+KT1L    = 0            KT2     = 0.022            UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11         AT      = 3.3E4
+WL      = 0            WLN     = 1                WW      = 0
+WWN     = 1            WWL     = 0                LL      = 0
+LLN     = 1            LW      = 0                LWN     = 1
+LWL     = 0            CAPMOD  = 2                XPART   = 0.5
+CGDO    = 6.52E-10     CGSO    = 6.52E-10         CGBO    = 1E-12
+CJ      = 1.157423E-3  PB      = 0.8444261        MJ      = 0.4063933
+CJSW    = 1.902456E-10 PBSW    = 0.8              MJSW    = 0.3550788
+CJSWG   = 4.22E-10     PBSWG   = 0.8              MJSWG   = 0.3550788
+CF      = 0            PVTH0   = 1.4398E-3        PRDSW   = 0.5073407
+PK2     = 2.190431E-3  WKETA   = 0.0442978        LKETA   = -2.936093E-3
+PU0     = -0.9769623   PUA     = -4.34529E-11     PUB     = 1E-21
+PVSAT   = -50          PETA0   = 1.002762E-4      PKETA   = -6.740436E-3    )
*
```

Example

Determine the resistance and capacitance of a Poly interconnect that is 0.6u wide and 800u long and compare that with the same interconnect if M_1 were used. Consider both 0.5u and 0.18u processes.

800μ

$$R_{POLY} = n_{SQ} R_{SH}$$

$$C_{P\text{-}SUB} = A \bullet C_{DPS}$$

$$R_{SH} = ?$$

$$C_{DPS} = ?$$

For 0.5u process

SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

R_{SH}=23.5Ω/□

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.5	105.3	23.5	999	44.2	0.09	0.11	ohms/sq
Contact Resistance	64.9	149.7	17.3		29.2		0.97	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	824	816	ohms/sq
Contact Resistance	0.79			ohms

COMMENTS: N\POLY is N-well under polysilicon.

C_{DPS}=84 af/μ^2

Note: substrate for p+ is the n-well

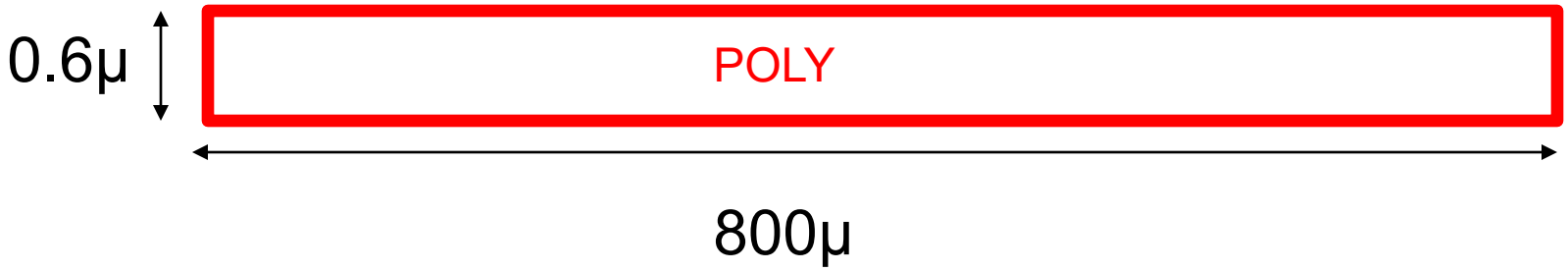
CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	aF/um^2
Area (N+active)			2434		35	16	11		aF/um^2
Area (P+active)			2335						aF/um^2
Area (poly)				938	56	15	9		aF/um^2
Area (poly2)					49				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							35		aF/um^2
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts

Example

For 0.5u process

Determine the resistance and capacitance of a Poly interconnect that is 0.6u wide and 800u long and compare that with the same interconnect if M_1 were used.



$$n_{SQ} = \frac{800\mu}{0.6\mu} = 1333$$

$$A = (0.6\mu)(800\mu) = 480\mu^2$$

$$R_{POLY} = n_{SQ} R_{SH} = 23.5 \cdot 1333 = 31.3K\Omega$$

$$C_{P\text{-}SUB} = A \cdot C_{DPS} = 480\mu^2 \cdot 84aF\mu^{-2} = 40.3fF$$

For 0.18u process

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms

R_{SH}=7.7Ω/□

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

C_{DPS}=103 af/μ²

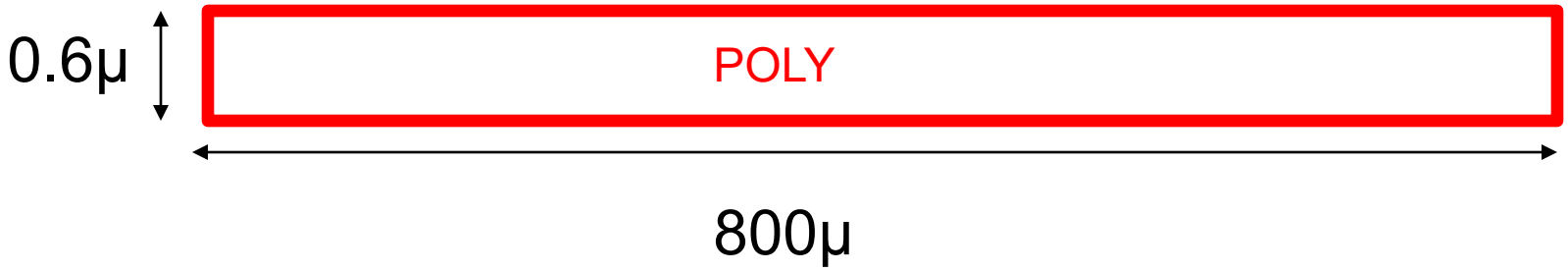
Note: substrate for p+ is the n-well

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

Example

For 0.18u process

Determine the resistance and capacitance of a Poly interconnect that is 0.6u wide and 800u long and compare that with the same interconnect if M_1 were used.



$$n_{SQ} = \frac{800\mu}{0.6\mu} = 1333$$

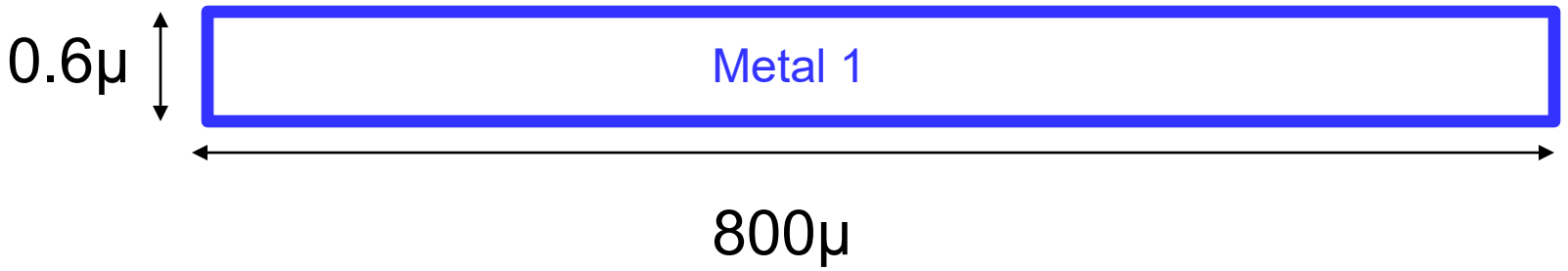
$$A = (0.6\mu)(800\mu) = 480\mu^2$$

$$R_{POLY} = n_{SQ} R_{SH} = 7.7 \bullet 1333 = 10.3K\Omega$$

$$C_{P\text{-}SUB} = A \bullet C_{DPS} = 480\mu^2 \bullet 103aF\mu^{-2} = 49.4fF$$

Example

Determine the resistance and capacitance of a Poly interconnect that is 0.6u wide and 800u long and compare that with the same interconnect if M_1 were used. Do this for both a 0.5u and a 0.18u process.



For 0.5u process

SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

R_{SH}=0.09Ω/□

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.5	105.3	23.5	999	44.2	0.09	0.10	ohms/sq
Contact Resistance	64.9	149.7	17.3		29.2		0.97	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	824	816	ohms/sq
Contact Resistance	0.79			ohms

COMMENTS: N\POLY is N-well under polysilicon.

C_{DPS}=27 af/μ^2

Note: substrate for p+ is the n-well

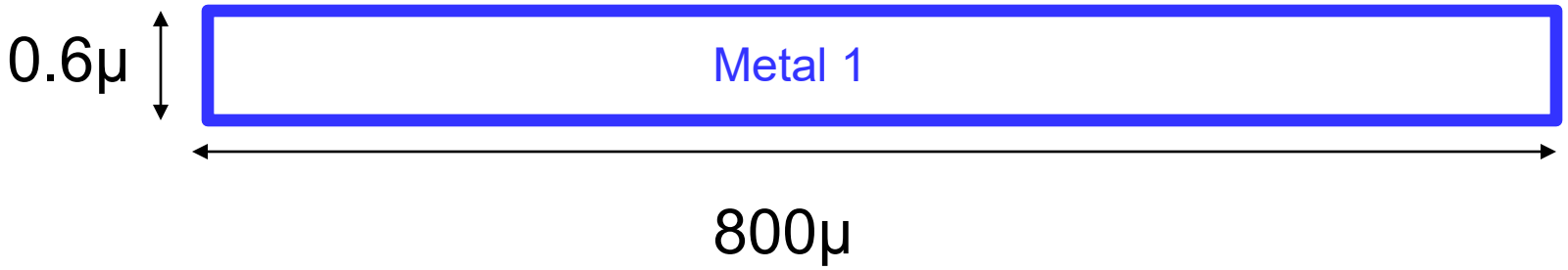
CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	aF/um^2
Area (N+active)			2434		35	16	11		aF/um^2
Area (P+active)			2335						aF/um^2
Area (poly)				938	56	15	9		aF/um^2
Area (poly2)					49				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							35		aF/um^2
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts

Example

For 0.5u process

Determine the resistance and capacitance of a Poly interconnect that is 0.6u wide and 800u long and compare that with the same interconnect if M_1 were used.



$$n_{SQ} = \frac{800\mu}{0.6\mu} = 1333$$

$$A = (0.6\mu)(800\mu) = 480\mu^2$$

$$R_{M1} = n_{SQ} R_{SH} = 0.09 \bullet 1333 = 120\Omega$$

$$C_{M1\text{-}SUB} = A \bullet C_{DM1S} = 480\mu^2 \bullet 27aF\mu^{-2} = 13.0fF$$

For 0.18u process

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms

R_{SH}=0.08Ω/□

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

C_{DPS}=39 af/μ²

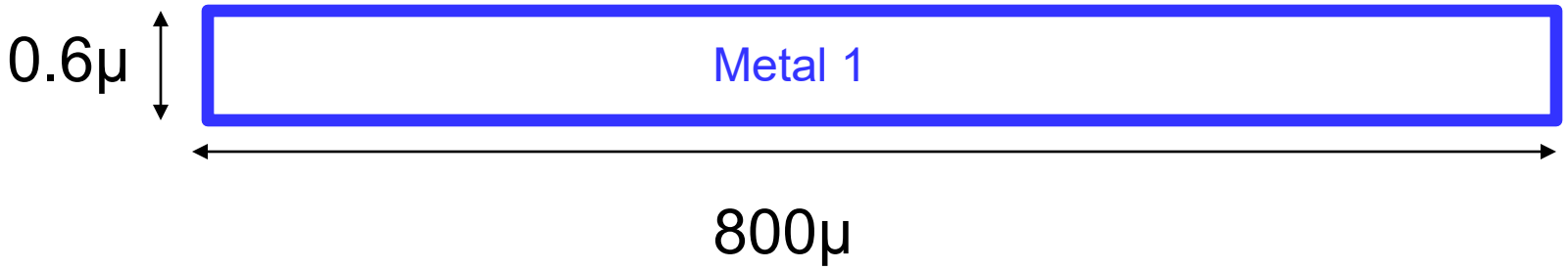
Note: substrate for p+ is the n-well

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

Example

For 0.18u process

Determine the resistance and capacitance of a Poly interconnect that is 0.6u wide and 800u long and compare that with the same interconnect if M_1 were used.



$$n_{SQ} = \frac{800\mu}{0.6\mu} = 1333$$

$$A = (0.6\mu)(800\mu) = 480\mu^2$$

$$R_{M1} = n_{SQ} R_{SH} = 0.08 \bullet 1333 = 107\Omega$$

$$C_{M1\text{-}SUB} = A \bullet C_{DM1S} = 480\mu^2 \bullet 39aF\mu^{-2} = 18.7fF$$

Example

Compare the resistance and capacitance of a n+ diffusion interconnect that is 0.6u wide and 800u long with what would be obtained with a Poly and a M_1 interconnet. Assume a 0.5u process.

800μ

$$R_{Diff} = n_{SQ} R_{SH}$$

$$C_{Diff\text{-}SUB} = A \bullet C_{D\_Diff\text{-}SUB}$$

$$R_{SH} = ?$$

$$C_{D\_Diff\text{-}SUB} ?$$

For 0.5u process

SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

R_{SH}=83.5Ω/□

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.5	105.3	23.5	999	44.2	0.09	0.10	ohms/sq
Contact Resistance	64.9	149.7	17.3		29.2		0.97	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	824	816	ohms/sq
Contact Resistance	0.79			ohms

COMMENTS: N\POLY is N-well under polysilicon.

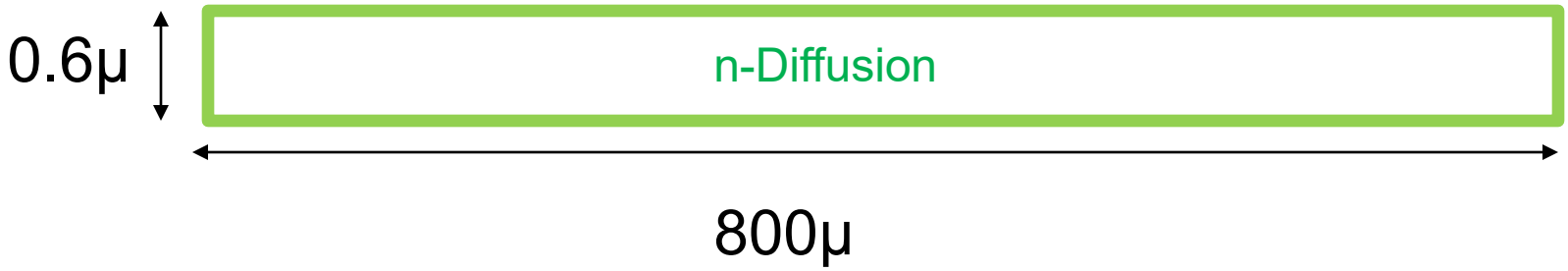
C_{DPS}=425 af/μ²

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	aF/um^2
Area (N+active)			2434		35	16	11		aF/um^2
Area (P+active)			2335						aF/um^2
Area (poly)				938	56	15	9		aF/um^2
Area (poly2)					49				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							35		aF/um^2
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts

Example

Compare the resistance and capacitance of a n+ diffusion interconnect that is 0.6u wide and 800u long with what would be obtained with a Poly and a M_1 interconnet. Assume a 0.5u process.



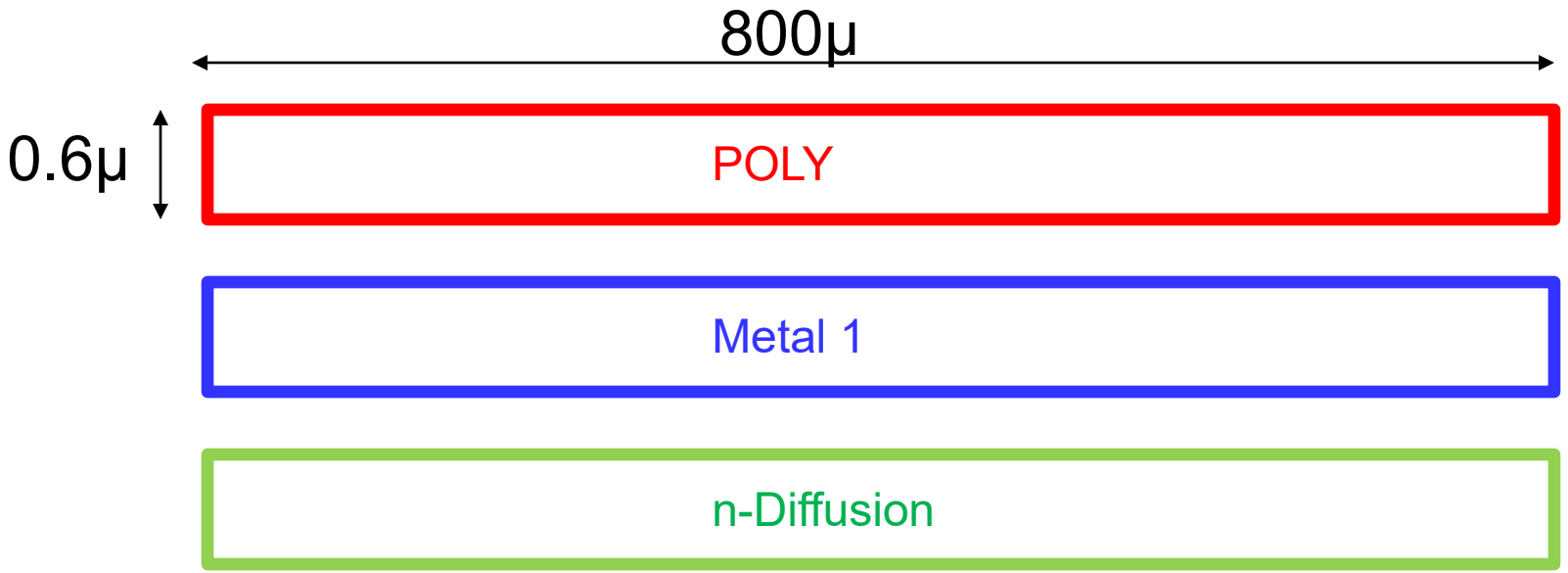
$$n_{SQ} = \frac{800\mu}{0.6\mu} = 1333$$

$$A = (0.6\mu)(800\mu) = 480\mu^2$$

$$R_{n+} = n_{SQ} R_{SH} = 83.5 \bullet 1333 = 111K\Omega$$

$$C_{n+\text{-}SUB} = A \bullet C_{Dn+S} = 480\mu^2 \bullet 425aF\mu^{-2} = 204fF$$

Comparison of 3 types of interconnects



		Poly 1	M1	Diff
0.18u	**R**	10.3K	107	8.8K
	C	49.4fF	18.7fF	479fF
0.5u	**R**	31.3K	120	111K
	C	40.3fF	13fF	204fF

Stay Safe and Stay Healthy !

End of Lecture 11